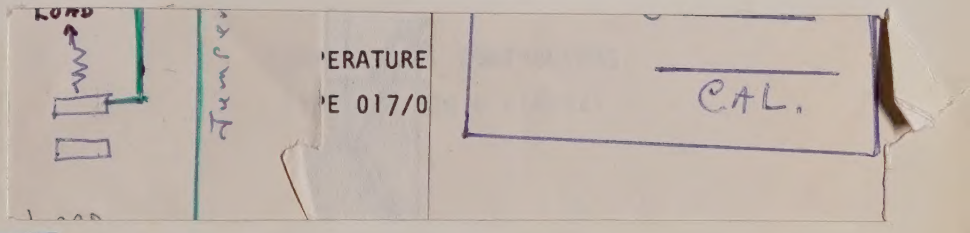
0197

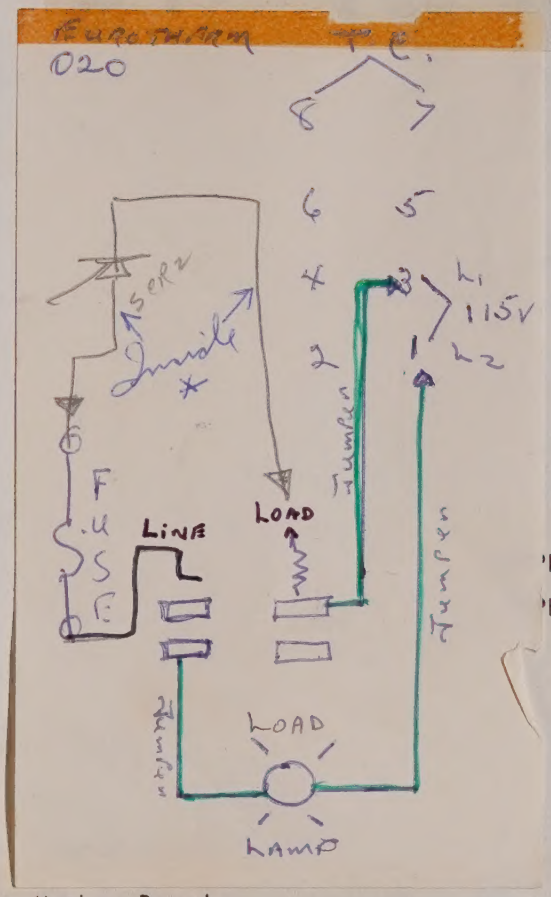
EUROTHERM Industrial Control Equipment

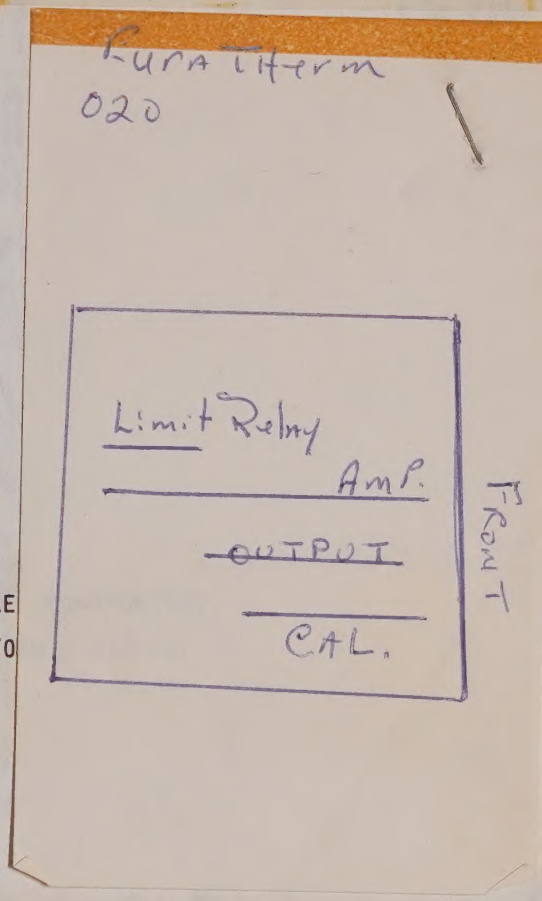
0197



Hook up
See Inside of
this Cover. →

0197

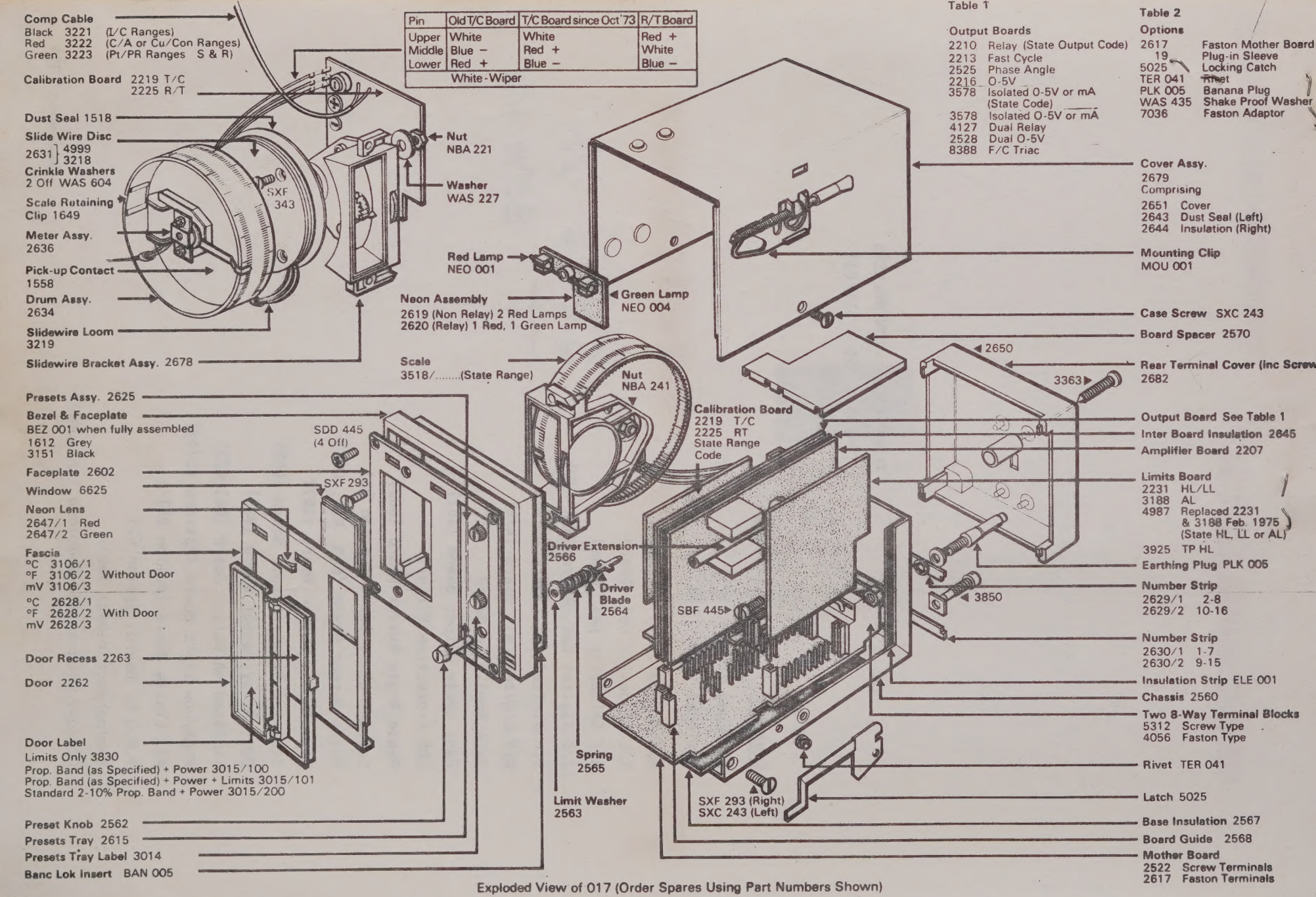




ERATURE
E 017/0

Mother Board
T/C Slidewire Cal. Board
R/T Slidewire Cal. Board
T/C Digital Cal. Board (Non K/V)
T/C Digital Cal. Board (K/V)
R/T Digital Cal. Board (K/V)
Main Amplifier Board
Fast Cycle Output Board (001)
SCR Protection Circuit
Phase Angle Output Board (002)
Current Limit Board (Option 42)
Relay Output Board (003, 026, 028)
Dual 5-volt Output Board (007)
Isolated 5-volt Output Board (008)
Dual Relay Output Board (023)
Isolated mA Output Board (067-073)
High/Low Limit Board (Options 02/03)
All Limits Board (Option 04)
T.P.H.L. Board (Option 67)
Semiconductor Data Table
Circuit Diagram for Complete Instrument

SCR's up to 25 Amps.



Pin	Old T/C Board	T/C Board since Oct '73	R/T Board
Upper	White	White	Red +
Middle	Blue −	Red +	White
Lower	Red +	Blue −	Blue −
	White - Wiper		

Table 1

Output Boards

2210	Relay (State Output Code)
2213	Fast Cycle
2525	Phase Angle
2216	O-5V
3578	Isolated 0-5V or mA (State Code)
3578	Isolated O-5V or mA
4127	Dual Relay
2528	Dual O-5V
8388	F/C Triac

Table 2

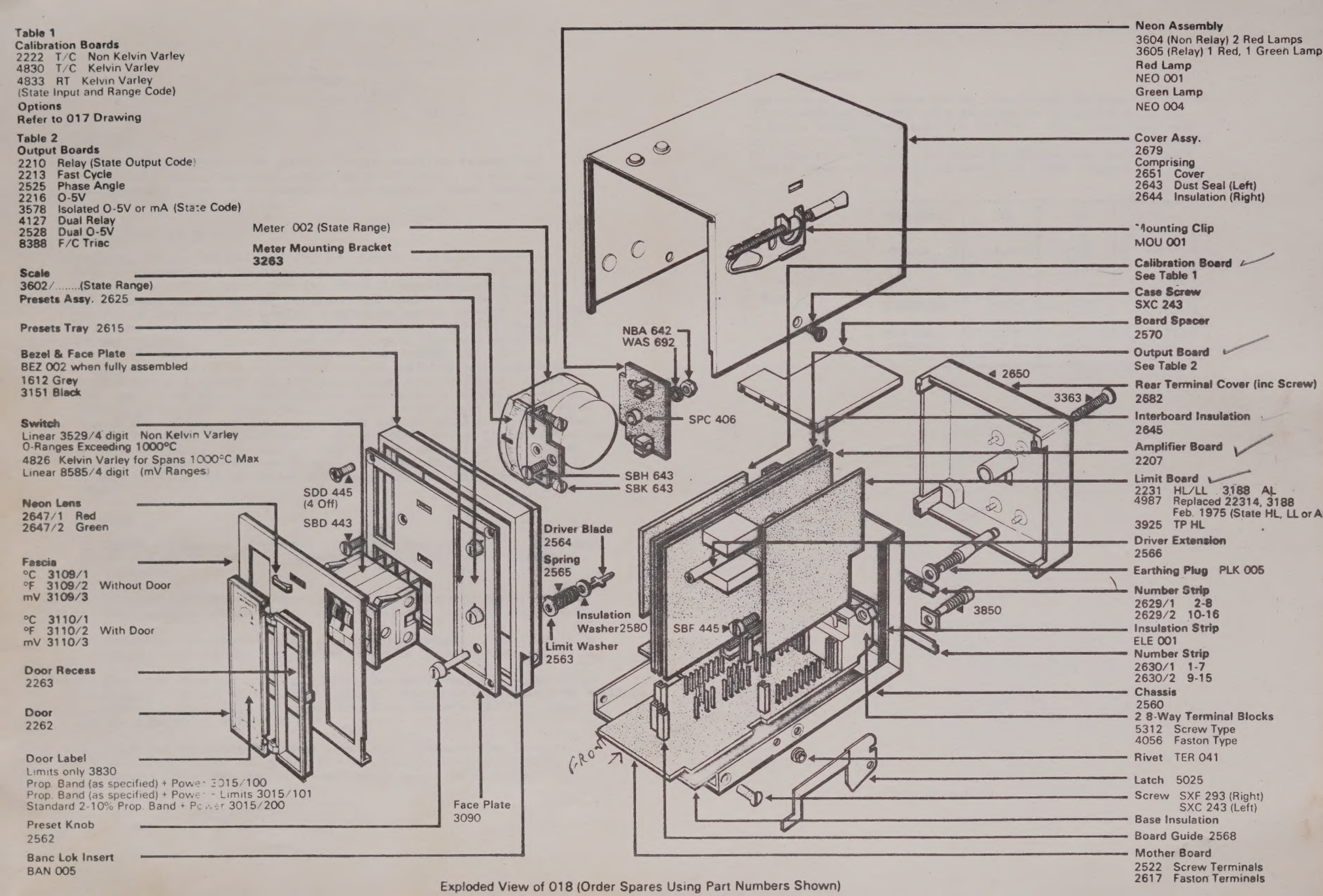
Options

2617	Faston Mother Board
19	Plug-in Sleeve
5025	Locking Catch
TER 041	Rivet
PLK 005	Banana Plug
WAS 435	Shake Proof Washer
7036	Faston Adaptor

Exploded View of 017 (Order Spares Using Part Numbers Shown)

Table 1
Calibration Boards
2222 T/C Non Kelvin Varley
4830 T/C Kelvin Varley
4833 RT Kelvin Varley
(State Input and Range Code)
Options
Refer to 017 Drawing

Table 2
Output Boards
2210 Relay (State Output Code)
2213 Fast Cycle
2525 Phase Angle
2216 O-5V
3578 Isolated O-5V or mA (State Code)
4127 Dual Relay
2528 Dual O-5V
8388 F/C Triac



Exploded View of 018 (Order Spares Using Part Numbers Shown)

MOTHER BOARD

Function

The mother board provides the necessary interconnections between the plug-in calibration, amplifier, output and alarm boards. It also carries the components necessary for generating the instrument power supplies and for driving the deviation meter.

Circuit Description

A smooth, isolated unstabilised -28V d.c. supply is obtained across C2 from the centre-tapped transformer secondary via diodes D2, D4, D5. Full-wave rectification is provided by D2, D4 and D5 effectively isolates the -28V smoothed supply from the -24V unsmoothed supply. Diodes D1, D3 provide an unsmoothed +24V supply. A reference voltage of -8.2V is provided at T3 base by the zener diode Z1 mounted on the main amplifier board. Emitter follower T3 uses this reference voltage to provide a stabilised -9V supply at the emitter via the emitter load resistor R10. The stabilised -4V supply is derived from the main amplifier board components Z1, T13 with mother-board resistor R8 acting as an emitter load for T13. The signal to the temperature indicating error meter is required to remain constant as the proportional band is altered. Connection of the error meter between the -4V supply and the wiper of the main amplifier proportional band control P1 fulfils this requirement. The emitter followers T1, T2 are included to prevent the meter from loading P1 and the -4V common line. Resistor R6 provides base current drive to T2 so that this current is not drawn from P1. Transistors T1 and T2 are matched for Vbe to minimise temperature drift and offset.

Checking

1. Insert the main amplifier board into the mother board in order to obtain the -4V and -9V supplies. Connect the mains supply to the appropriate terminals.

2. Check the +24V and -24V unsmoothed supplied with a d.c. voltmeter. If these supplies are not present check transformer TX1 and diodes D1 to D4.

3. Check the -28V smoothed supply with a d.c. voltmeter. If this supply is not present check diode D5. If the supply is low check capacitor C2.

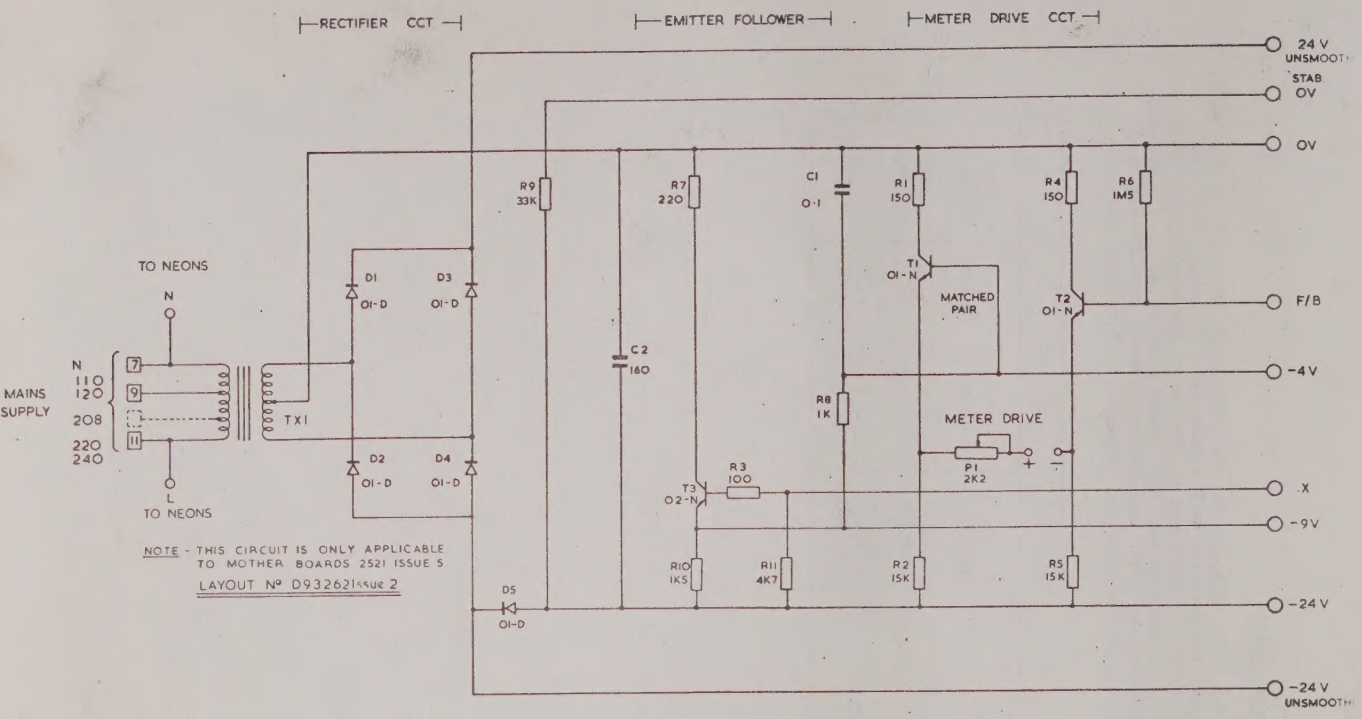
4. Check the -9V stabilised supply with a d.c. voltmeter, this normally lies between -8.5V and -9.3V. If this supply is incorrect check that a -8.2V ±5% reference is available at T3 base from Z1 on the main amplifier, then check operation of T3.

5. Check the -4V stabilised supply with a d.c. voltmeter, this normally lies between -3.8V and -4.2V. If this supply is incorrect check Z1 and T13 on the main amplifier board and T3 on the mother board.

D.C. Voltage Table.

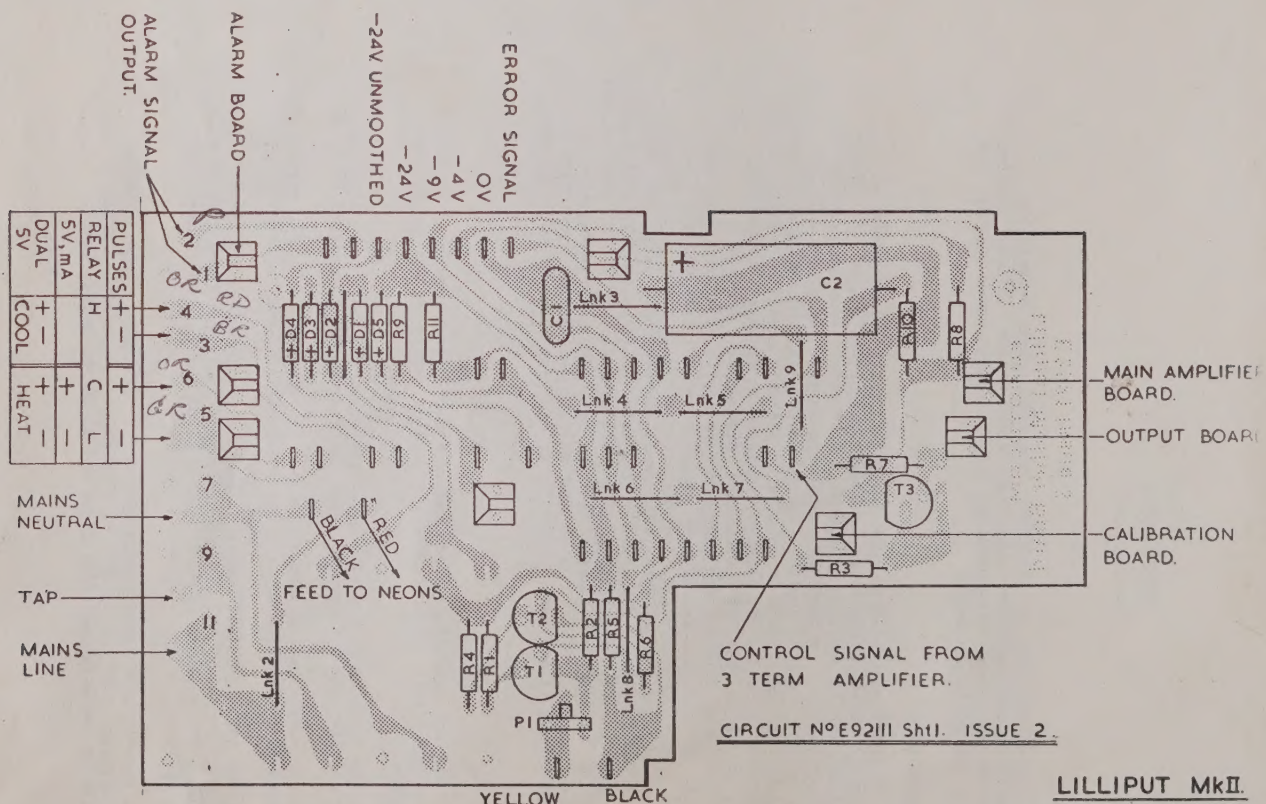
Typical d.c. test voltages for the transistors are shown in the table. All voltages are measured with reference to 0V using a 10V d.c. voltmeter having a resistance of 20KΩ/volt. The proportional band control, P1 on the main amplifier board, must be set to its maximum fully-clockwise position. Voltages are checked with the indicator upscale (over temperature) and downscale (under temperature).

	INDICATOR	T1	T2	T3
EMITTER	UPSCALE	-4.6v	-5.5v	-9v
	DOWNSCALE	-2 v	-1 v	-9v
BASE	UPSCALE	-4 v	-7.7v	-8v
	DOWNSCALE	-4 v	-.3 v	-8v
COLLECTOR	UPSCALE	-.5 v	o v	-1.5v
	DOWNSCALE	o v	-o.5v	-1.2v



LILLIPUT Mk II.
MOTHER BOARD.

Drg Nº E92111 Sht 1



CIRCUIT Nº E92111 Sht1. ISSUE 2.

LILLIPUT MkII.
MOTHER BOARD.

Drg Nº D93262 Issue2

SLIDEWIRE THERMOCOUPLE CALIBRATION BOARD.

Function

The thermocouple slidewire calibration board subtracts the thermocouple e.m.f. from the slidewire reference voltage and feeds the resultant error signal to the main amplifier inputs A and B.

Circuit Description.

The required millivolt span of the controller is developed across the slidewire by the current defined by R1, P1. The thermocouple e.m.f. is subtracted from the slidewire reference voltage and the error difference is fed to the amplifier input A via R5. The filter C1, R5 rejects mains frequency series mode interference at the thermocouple input. Potentiometer P3 gives fine calibration trim at the low end of the slidewire by developing a small voltage across R6 due to current through R8. Resistor R10 is fitted for negative temperature ranges only and is normally omitted. Resistor R2 may be fitted in place of a link to allow calibration at the low end of the slidewire to be within the range of the zero potentiometer. With the proportional band potentiometer at maximum the gain of the error amplifier is given by(R9 + R6)/R6 and is dependent on the span of the controller. The negative temperature coefficient thermistor R4, in association with components R3, P2. R7, provides automatic cold junction compensation by causing the voltage across R6 to rise slightly as the ambient temperature rises, due to the thermistor change of resistance from 13k at 30°C to 6k at 50°C.
Note: R1, R9 and R10 occasionally have a parallel resistor in order to obtain close adjustment.

Calibration Procedure (T/C 017 & 020)

1. Place controller on level surface with mains switched off and set meter mechanical zero by moving the spring-loaded magnet retainer.
2. Set Pot P1 on the mother board to minimum resistance (clockwise) to give maximum meter sensitivity during calibration and connect a compensated mV source such as Eurotherm Model 039 (see note below) with the correct compensating lead to the controller, observing the polarity.
3. Switch on the mains and allow the instrument and mV source to warm up for 20 minutes.
4. Set the cold junction compensation in the following manner:-
Turn the C.J.C. Pot P2 fully anti-clockwise onto the metal leg, short the thermistor R4 and inject the C.J.C. mV according to the type of thermocouple -

Iron/Con J	5.56 mV	For other thermocouples
NiCr/NiAl K	4.38 mV	mV = 5.35 (mV at 50°C - mV at 30°C)
Cu/Con T	4.49 mV	obtained from the temperature
Pt10%RhVPt S	0.67 mV	e.m.f. tables.
Pt13%Rh/Pt R	0.67 mV	

Null the deviation meter by moving the drum. Reduce C.J.C. mV to zero and renull the deviation meter by Pot P2. Remove thermistor short.
For ranges where moving the drum will not null the meter, select a mV figure which will, and then subtract the figure in the table instead of reducing the mV to zero. Renull the meter with potentiometer P2. Remove thermistor short.
5. Set zero in the following manner:- Select thermocouple type on the 039,inject mV equivalent to bottom end of scale temperature and with the drum set to minimum setting null the deviation meter by means of Pot P3.
6. Set span in the following manner:- inject full scale mV and with the drum set to full scale null the deviation meter by means of Pot P1.
7. Repeat 5 and 6 until no further adjustment is necessary.
8. Set drum to midspan position and inject the corresponding mV. Dial set points 5% above and 5% below the injected signal and adjust by P1 on the mother board until the meter follows the scale.
9. Check thermocouple break protection by disconnecting one of the input leads and observing the indicator going upscale (or downscale if that option is on the instrument).

Note:- If the calibrator is an uncompensated potentiometer a cold-junction correction must be made when setting the maximum and minumum signals on the potentiometer. The cold junction appears at the potentiometer terminals and a thermometer is usually located adjacent to these terminals for corrected purposes. Read the temperature on this thermometer and obtain the equivalent millivolts from the thermocouples tables. Read the millivolt figures equivalent to maximum and minimum controller temperatures and subtract the cold junction millivolts from each of these figures. Use the corrected figures to calibrate the controller as described above. If the minimum controller temperature is 0°c the subtraction gives a negative figure. Calibration at 0°c is achieved by reversing the polarity of the compensating lead at the potentiometer terminals and setting the potentiometer to the cold junction millivolts. Remember to reconnect the compensating lead in the correct polarity when making the maximum temperature adjustment. No correction is required for thermocouple lead resistance.

Checking

1. Check the faston connections to the slidewire.Note: the connections are different on the new version of the calibration board.Check the resistance of the slidewire with a resistance meter. This should be approximately 21 ohms.
2. Check the faston connections to the rear terminal block and check the resistance of the thermocouple. This should be less than 100 ohms.
3. Check the -4V supply to the calibration board. Note that the main amplifier board must also be plugged in to the mother board.
4. If the calibration board has to be replaced, adjust the cold junction compensation and the calibration as described.

CALIBRATION BOARD COMPONENTS FOR T/C 017 020 INSTRUMENTS
(- means open circuit)

J Iron/Con BS 4937 and ASTM E230-72 (Black Comp cable + wire yellow - wire blue)

CODE	RANGE	R1	R13	R2	R12	R7	R9	R11	R10	R15	R14	P1
01 015	0-100°C	12K	-	5.6Ω	-	1K2	56K	470K	-	-	-	4K7
01 017	0-200°C	6K2	-	2.2Ω	-	1K2	24K	-	-	-	-	2K2
01 018	0-250°C	5K6	-	1.5Ω	-	1K2	22K	150K	-	-	-	1K
01 020	0-400°C	3K	-	0.5Ω	-	1K2	12K	-	-	-	-	1K
01 023	0-600°C	2K2	-	LINK	-	1K2	8K2	330K	-	-	-	470Ω
01 024	0-800°C	1K5	-	LINK	-	1K2	6K8	39K	-	-	-	470Ω
01 059	250-450°C	6K2	-	22Ω	-	1K2	24K	-	-	-	-	2K2
01 096	0-300°C	4K3	-	1Ω	-	1K2	18K	180K	-	-	-	1K
01 115	32-600°F	3K9	-	1Ω	-	1K2	15K	-	-	-	-	1K
01 116	32-400°F	6K2	-	2.2Ω	-	1K2	24K	-	-	-	-	2K2
01 119	32-800°F	2K7	-	0.5Ω	-	1K2	12K	-	-	-	-	1K
01 125	32-1400°F	1K6	-	LINK	-	1K2	6K2	-	-	-	-	470Ω
01 131	-25 to +25°C	15K	180K	LINK	-	1K2	56K	-	-	-	-	5K short scale
01 134	0-400°F	6K2	-	3.3Ω	-	1K2	22K	-	-	-	-	1K
01 144	100-300°C	6K8	-	12Ω	330K	1K2	24K	-	-	-	-	1K
01 190	200-400°C	6K8	-	22Ω	-	1K2	24K	-	-	-	-	1K

Iron/Con DIN 43710 Black Comp.Cable + wire Yellow - Wire Blue

CODE	RANGE	R1	R13	R2	R12	R7	R9	R11	R10	R15	R14	P1
02 017	0-200°C	6K2	-	2.2Ω	-	1K2	24K	-	-	-	-	2K2
02 020	0-400°C	3K	-	0.5Ω	-	1K2	12K	-	-	-	-	1K
02 023	0-600°C	2K2	-	LINK	-	1K2	8K2	330K	-	-	-	470Ω
02 096	0-300°C	4K3	-	1Ω	-	1K2	18K	180K	-	-	-	1K

K C/A BS4937 ASTM 230-72 Red Comp. Cable + Wire White - Wire Blue

03 003	-100- +100°C	9K1	-	3.3Ω	-	1K8	33K	-	39K	-	-	2K2
03 006	-50 - +150°C	9K1	-	LINK	-	1K8	33K	-	220K	-	-	2K2
03 012	-3 - +3mV	10K	-	LINK	-	1K8	47K	-	82K	-	-	4K7
03 017	0-200°C	8K2	-	2.2Ω	-	1K8	33K	-	-	-	-	2K2
03 020	0-400°C	4K3	-	1Ω	-	1K8	15K	-	-	-	-	1K
03 023	0-600°C	2K7	-	0.5Ω	-	1K8	10K	-	-	-	-	1K
03 024	0-800°C	2K	-	LINK	-	1K8	8K2	-	-	-	-	470Ω
03 026	0-1200°C	1K3	-	LINK	-	1K8	5K6	-	-	-	-	470Ω
03 068	-100 - +400°C	3K3	-	LINK	-	1K8	12K	-	-	-	-	1K
03 069	-100°C- +500°C	2K7	-	LINK	-	1K8	11K	-	39K	-	-	1K
03 075	-50° - 600°C	2K2	-	LINK	-	1K8	10K	-	75K	-	-	1K
03 090	-200 - +200°C	5K1	-	LINK	-	1K8	18K	-	-	-	-	1K
03 096	0-300°C	5K6	-	1Ω	-	1K8	22K	-	-	-	-	1K
03 116	32-400°F	8K2	-	LINK	-	1K8	33K	-	-	-	-	2K2
03 119	32-800°F	3K3	-	LINK	-	1K8	15K	-	-	-	-	1K
03 124	32-1200°F	2K4	-	LINK	-	1K8	10K	-	-	-	-	1K
03 126	32-1600°F	1K6	-	LINK	-	1K8	7K5	-	-	-	-	1K
03 127	32-1650°F	1K8	-	LINK	-	1K8	6K8	-	-	-	-	1K
03 132	32-2200°F	1K3	-	LINK	-	1K8	5K6	-	-	-	-	470Ω

T Cu/Con BS4937 ASTM E230-72 Red or Blue Comp.Cable + Wire White - Wire Blue

04 003	-100- +100°C	9K1	-	LINK	-	1K8	33K	-	62K	-	-	2K2
04 017	0-200°C	7K5	-	2Ω2	-	1K8	27K	-	-	-	-	1K
04 020	0-400°C	3K	-	2Ω2	-	1K8	12K	-	-	-	-	1K
04 072	-50-100°C	12K	-	LINK	-	1K8	47K	-	-	-	-	2K2
04 096	0-300°C	4K7	-	2Ω2	-	1K8	18K	-	-	-	-	1K
04 135	-200- +250°C	3K9	-	LINK	-	1K8	15K	-	24K	-	-	1K
04 137	-200 - 0°C	12K	-	LINK	-	1K8	47K	-	33K	-	-	4K7

R Pt13%Rh-Pt BS4937 ASTME230-72 Green Comp.Cable + Wire White - Wire Blue

05 026	0-1200°C	5K1	-	LINK	-	8K2	22K	-	-	-	-	1K
05 028	0-1600°C	3K6	-	LINK	-	8K2	15K	-	-	-	-	1K
05 136	32-2900°F	3K6	-	LINK	-	8K2	15K	-	-	-	-	1K

S Pt10% Rh-Pt BS4937 ASTM E230-72 Green Comp.Cable + Wire White - Wire Blue

06 026	0-1200°C	5K6	-	LINK	-	8K2	22K	-	-	-	-	1K
06 028	0-1600°C	3K9	-	LINK	-	8K2	15K	-	-	-	-	1K
06 036	32-2900°F	3K9	-	LINK	-	8K2	15K	-	-	-	-	1K

Pt 20% Rh - Pt5%Rh Johnson Matthey Cu Wires. 15K instead of thermistor.

CODE	RANGE	R1	R13	R2	R12	R7	R9	R11	R10	R15	R14	P1
07 029	0-1800°C	5K6	-	2Ω2	-	1K8	22K	-	-	-	-	1K

B Pt30%Rh-Pt6%Rh BS4937 ASTM E230-72 Cu.Wires 15K instead of thermistor

08 029	0-1800°C	5K1	-	2Ω2	-	1K8	18K	-	-	-	-	1K

W/W26%Re Engelhard Cu Wire CJC inject is 0.335mV

09 066	0-2000°C	1K5	-	LINK	-	47K	7K5	-	150K	-	-	1K

1R/1R 40% Re. Engelhard Cu. Wire. The thermistor is left in.

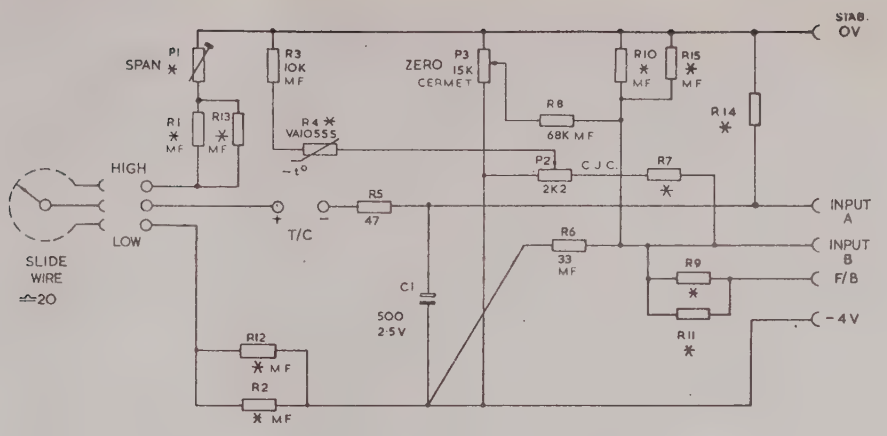
18 044	1000-1800°C	15K	-	27Ω	-	8K2	68K	-	-	-	-	4K7

LAND PYROMETER Q003 Cu.Wires.15K instead of Thermistor.Fit 500Ω across pins 15 & 1

51 081	0-1400°C	1K3	-	LINK	-	1K2	5K1	-	-	-	-	470Ω
51 123	0-1300°C	2K4	-	LINK	-	O/C	10K	-	-	-	-	470Ω

Pt 20% Rh/Pt 40% Rh Johnson Matthey Cu.Wire 15K instead of Thermistor

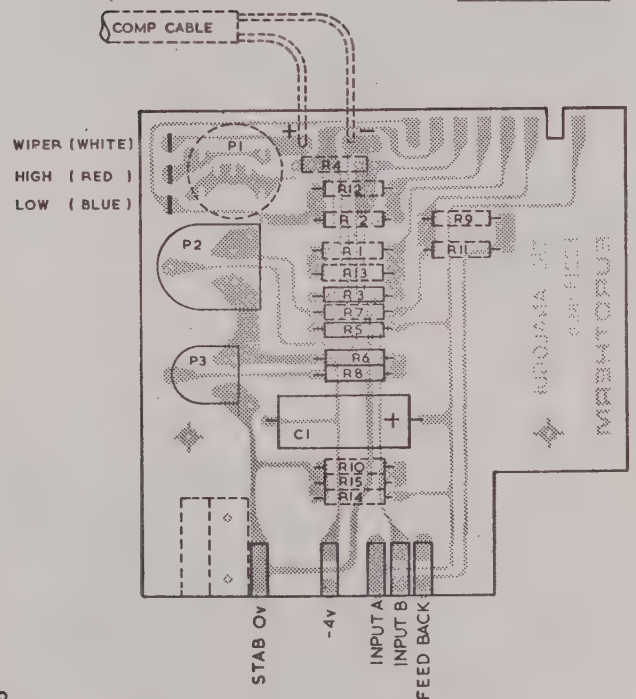
25 143	800-1800°C	18K	-	4Ω7	-	8K2	68K	-	-	-	-	4K7



COMPONENTS SHOWN THUS * VARY WITH THERMOCOUPLE AND SCALE RANGE.
REFER TO WRITE UP FOR DETAILS.

LILLIPUT MkII.
SLIDEWIRE T/C CAL BOARD.
LAYOUT Nº D93165

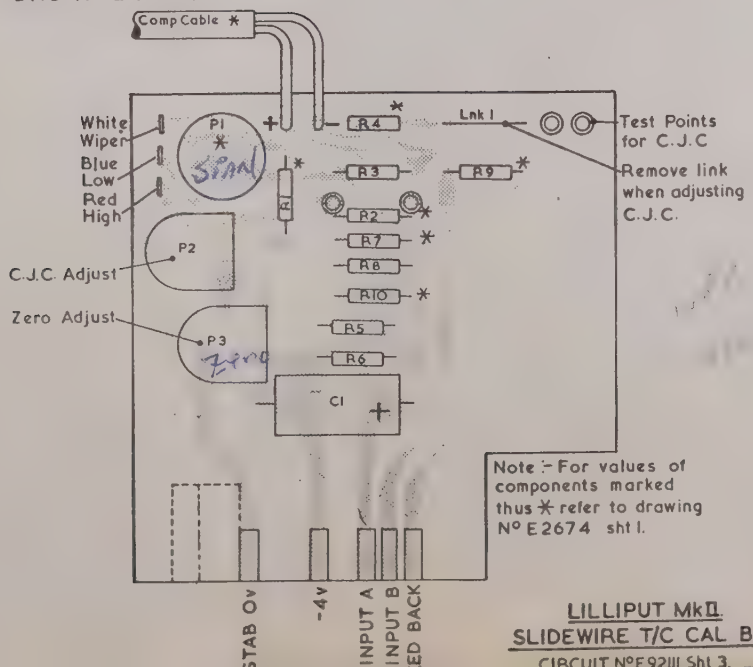
Drg Nº E92111 Sht 3



017 T/C
CAL BOARD,

Circuit Nº E 92111
sheet 3.

DRG Nº E 92219



LILLIPUT MkII.
SLIDEWIRE T/C CAL B'd.
CIRCUIT Nº E 92111 Sht 3.

SLIDEWIRE RESISTANCE THERMOMETER CALIBRATION BOARD.

Function.

The platinum resistance thermometer slidewire calibration board effectively subtracts the voltage drop across the resistance thermometer from the slidewire reference voltage to produce an error signal. These voltages are fed to the main amplifier input A and B.

Circuit Description.

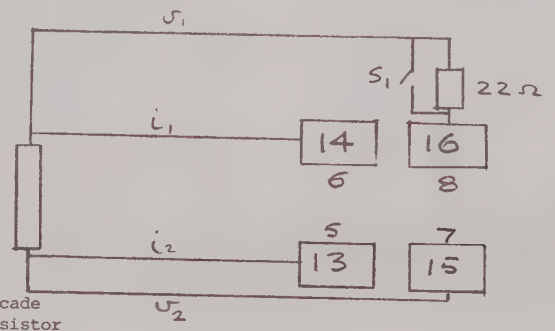
The required millivolt span of the controller, standardized at 25mV (was 40mV up to 1973) is developed across the slidewire by the current defined by R1 + P1. The control temperature is set by tapping the reference voltage from the slidewire and this voltage is applied to input A of the main amplifier via R4.
The voltage developed across the resistance thermometer by the nearly constant resistance thermometer current is applied to input B of the main amplifier via R8. The resistance thermometer voltage is thus effectively subtracted from the reference voltage.
The current flowing through the resistance thermometer is defined by R5.
At 0°C, the thermometer has a resistance of 100 ohms and offset of the reference voltage is required for zero adjustment. This offset is obtained by means of R2, R3 and P2. Potentiometer P3 is adjusted to eliminate current flow in the V1 wire by equalising the currents in R5 and R6. Resistor R7 reduces loading of the -9v rail.
Components R4, C1 form a filter to provide mains frequency series mode pick-up rejection and C2 provides high frequency interference rejection. Resistor R3 is fitted when zero offset spans are required. Resistors R9, R8 and the RT itself define the gain of the main amplifier, the required gain being dependent on the span of the controller. The RT as it varies will change the gain therefore the error meter sensitivity but this variation is small and acceptable.

Pt. 100 RT Calibration Board Values for 017

Code	Range	P1	P2	P3	R1 (RSY or RTY)	R2 (RTM)	R3 (RTM)	R5 (RSY or RTY)	R6 (RSY or RTY)	R7 (RSY or RTY)	R9 (RSS)
70-005	-50 to +50°C	470	100	2K2	3K//56K	150	50	6K2	6K8	18K	100K
70-200	-30 to +60°C	1K	100	2K2	3K6	600// 390	2K2	6K8	7K5	18K	100K
70-189	-70 to +200°C	470	100	4K7	3K	56	18// 100	16K	18K	18K	120K
70-015	0 to 100°C	470	100	4K7	3K3// 22K	120	68	6K2	5K6	18K	120K
70-017	0 to 200°C	470	100	10K	2K7	100	33// 270	12K	10K	18K	120K
70-096	0 to 300°C	470	100	22K	2K7	33	22// 220	18K	8K2	18K	150K
70-020	0 to 400°C	470	100	15K	2K7// 15K	15	15	22K	22K	18K	150K
70-024	0 to 800°C	470	470	10K	1K2	27	10// 22	12K	22K	82K	120K
70-133	0 to 50°F (3 RT in series)	220	100	2K2	3K3// 50K	680	270	5K1	5K6	18K	180K
70-114	32-200°F	470	100	10K	2K7	220	68	5K6	3K3	18K	120K

RTM = 0.5% 1/8W 50ppm metal film RSY & RTY = 2% 1/8W 70ppm metal oxide
RSS = 5% 1/8W 500ppm carbon film.

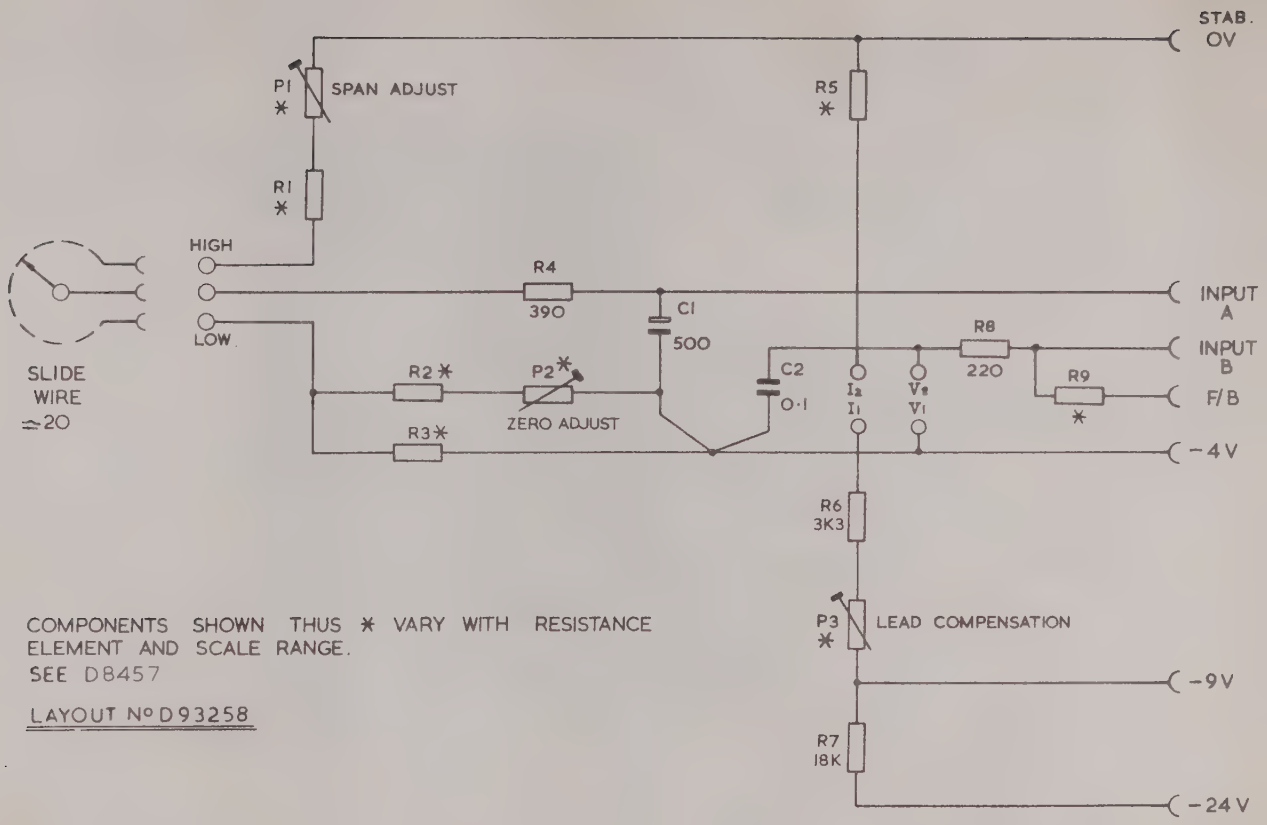
Note:- These values only apply when R8=220 ohm and R4=390 ohm. R2 and R3 may have to be selected on test and the above values are only for guidance.
R.T. Calibration:- Zero adjustment is made at minimum setting on drum:this may not be 0°C. Span adjustment is made at 80% of total range.
1. Place controller on a level surface with the mains switched off and set the meter mechanical zero by moving the spring-loaded magnet retainer.
2. Set pot P1 on the mother board to minimum resistance (clockwise) for maximum deviation meter sensitivity and connect the controller to a decade resistance box as in the diagram, with switch S1 shorting out the 22 ohm resistor. Place zero Pot P2 in the centre of its travel.
3. Set resistance corresponding to zero setting, on the decade box. With the drum in the zero position adjust the span Pot P1 to null the deviation meter.
4. Set resistance corresponding to span on the decade box. With the drum set to span position note error seen on deviation meter and with span pot move the deviation meter to read the same error, the opposite side of the null point. (e.g. if error is + 10°, move meter to read -10° from set point.)
5. Set resistance corresponding to zero on decade box and with drum set to zero, adjust zero Pot P2 to null deviation meter.
Repeat 4 and 5 until no further adjustment is necessary.
6. At span, adjust lead compensation Pot P3 to give no change on the meter when S1 is opened and closed. Close S1.
7. Set drum and decade resistor to 80% of span:check deviation meter sensitivity by dialling 5% downscale. If the meter does not follow the scale adjust Pot P1 on mother board until it does.
Note:- It is usual to reseal P1 and P2 to prevent movement.by vibration.



Terminal Nos.5,6,7 & 8 apply to models 020, 021.

Decade Resistor 0-999.9Ω ± 0.1%

Connections for Calibration of 017 or 018 with Pt RT Input.

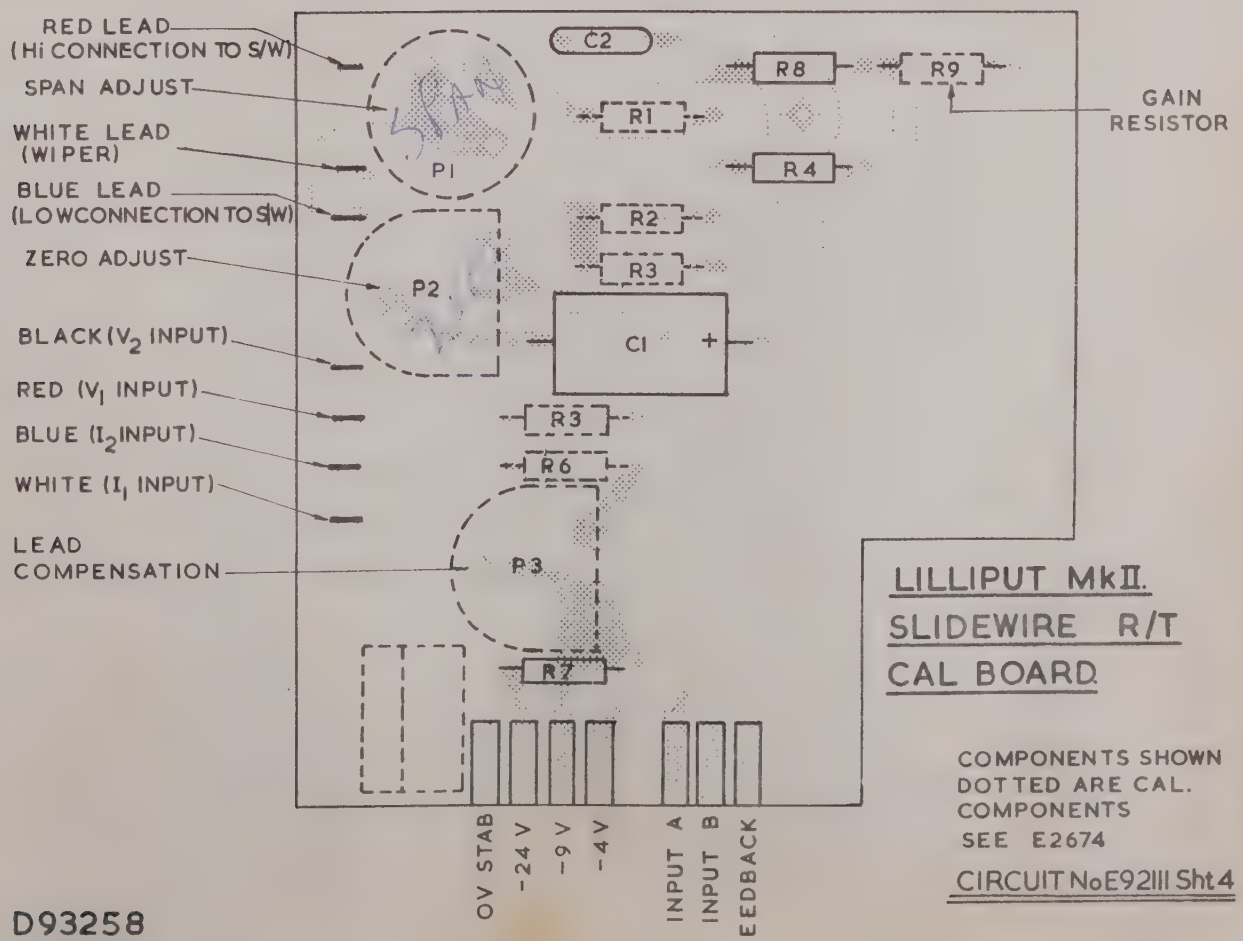


COMPONENTS SHOWN THUS * VARY WITH RESISTANCE ELEMENT AND SCALE RANGE.
SEE D8457

LAYOUT No D93258

LILLIPUT Mk II.
SLIDEWIRE R/T CAL B'd

Drg No E92111 Sht 4



LILLIPUT Mk II.
SLIDEWIRE R/T CAL BOARD

COMPONENTS SHOWN DOTTED ARE CAL. COMPONENTS
SEE E2674

CIRCUIT No E92111 Sht 4

D93258

DIGITAL (NON KELVIN - VARLEY) THERMOCOUPLE CALIBRATION BOARD.

Function.

The thermocouple digital calibration board subtracts the thermocouple e.m.f. from the digitally set, linearised reference voltage and feeds the resultant error signal to the main amplifier input.

Circuit description.

The reference voltage is obtained by digit switches S1 to S3 (S1 to S4 for four digits) tapping three (four) voltages from the resistor chain R1 to R10 (see drawings C92111, sheets 10, 11, 12(. These tapped voltages are scaled and added by resistors R11, R12, R13 and R14 .
Transistors T1 to T3 and associated components form a buffer amplifier to prevent loading of the reference circuit. After buffering, the amplified reference voltage is applied to a series of linearising circuits formed by transistors T4 to T9 and associated components. The linearising circuits modify the reference input from the digital switches to produce a characteristic which closely matches the particular thermocouple characteristic. This matching is obtained by applying cut (slope decrease) or lift (slope increase) to the low and high ends of the reference characteristic.
Transistors T4, T5 form a low cut circuit which decreases the slope of the reference characteristic at low values of reference voltage below a value defined by the bias on T5 base. Transistors T6, T7 form a second low cut circuit which modifies the slope of the reference characteristic for signal levels below the value defined by the bias on T7 base. Diodes D1, D2, and associated components form a gating circuit which provides low signal lift. Transistors T8, T9, provide either high signal lift or cut depending on the link configuration. The net current flowing in the linearising network is fed to the R32, R33 parallel combination to produce the required reference.
Automatic cold junction temperature compensation is provided by the negative temperature coefficient thermistor R35 in association with components R34, P3, R38. The voltage across R38 is caused to rise slightly as the ambient temperature rises. The required level of compensation is set on P3. Components R36, C4 form a series mode interference filter which rejects mains frequency pick-up at the thermocouple input.
Span adjustment is provided by P1 which defines the current flowing in the digit switch resistor chain R1 to R10. Zero adjustment is provided by P2 which allows a current bleed through R32, R33 via R30 to compensate for offset which may exist at the output of the linearising network. Resistor R40 defines the gain of the main amplifier, the required gain being dependent on the span of the controller.
Capacitors C1, C2, and C3 provide stabilisation of the amplifier and linearising circuits.

Calibration

1. Place the controller on a level surface and check that the deviation meter is at zero. If not, adjust the plastic screw at the side of the meter to reset the mechanical zero.

2. Connect mains supply and a compensated mV source, such as the Eurotherm Model 039, to the appropriate rear terminals.

3. Switch on the instrument and mV source, and allow a twenty minute warm-up period.

4. Set the meter sensitivity pot (P1 on the mother board) fully clockwise to minimum resistance. This gives maximum meter sensitivity during calibration.

5. Cold junction compensation (C.J.C.)
Turn the C.J.C. pot P3 fully clockwise. Short circuit the thermistor R35. Inject mV according to the following table:-

Thermocouple Type		mV
Iron/Con	J	5.56
Copper/Con	T	4.49
Chromel/Alumel	K	4.38
Pt.10%Rh/Pt	S	0.67
Pt.13%Rh/Pt	R	0.67

For any other thermocouple, mV = 5.35 (mV at 50°C - mV at 30°C).
Adjust the instrument digit switch to set the deviation meter to zero. Reduce the injected mV to zero, and turn P3 anti-clockwise until the meter is again at zero. Remove the short circuit from the thermistor.
For ranges where moving the digit switch will not null the meter, select a mV figure which will, and then subtract the figure in the table instead of reducing the mV to zero. Renull the meter with pot P3. Remove thermistor short.

6. For different scale ranges, the zero and span adjustments should be made at the calibration points given in the following table:-

Scale range	Zero adjustment calibration point.	Span adjustment or calibration point.
0-199°C	2°C (0mV)	199°C
0-399°C	2°C (0mV)	399°C
0-999°C	200°C	800°C
0-1199°C	200°C	1000°C
0-1599°C	500°C	1200°C
0-999°F	200°F	800°F
0-1199°F	100°F	1100°F
0-1999°F	400°F	1600°F
0-2999°F	32°F	2200°F

a. Zero pot adjustment.
Set the instrument digit switch to the tabulated value for the zero adjustment cal. point. Inject the corresponding mV. Note that for 0-199°C and 0-399°C scale ranges, the injected mV is 0mV. Adjust the zero pot P2 to set the deviation meter to zero.

b. Span pot adjustment.
Set the instrument digit switch to the tabulated value for the span adjustment cal. point.

Inject the corresponding mV. Adjust the span pot P1 to set the deviation meter to zero.

Repeat operations (a) and (b) until no further adjustment is necessary.

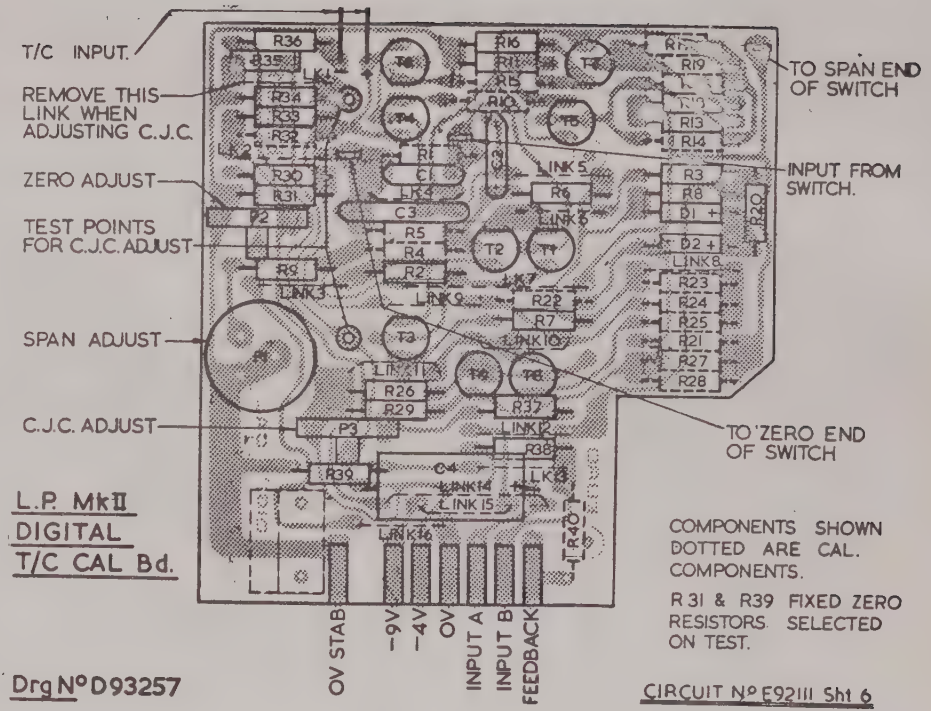
7. Meter sensitivity.

Set the instrument digit switch at 70% of span and inject the corresponding mV. Increase the instrument digit switch setting and adjust the meter sensitivity pot P1 on the mother board until the deviation meter gives an equivalent downscale indication.

8. Check thermocouple break protection by disconnecting one of the input leads and observing the indicator going upscale (or downscale if that option is called for).

Checking

1. Check all faston connections to the calibration board and check the resistance of the thermocouple. This should be less than 100 ohms.
2. Check the -4V supply to the calibration board. Note that the main amplifier board must also be connected to the mother board.
3. Disconnect the output of the digit switch assembly to the calibration board and connect a d.c. voltmeter between -4V supply and the switch output. Set the switches to zero and check that the output voltage is zero.
4. Increase the digit setting slowly up to the maximum value and check that equal increments of voltage occur at each decade. The switch resistor chain tappings provide 0.4V increments between 0 and +3.6V measured directly on the switch wipers.
Note:- In cases where the first digit is stopped at 1, e.g. 1200°C the 1 is normally taken to a higher tap on the resistor chain.
This ensures that adequate signal is always available for the reference circuit without recourse to increased gain in the calibration board, buffer amplifier. Therefore, the maximum output from the digit switch will vary with different spans. The amplifier gain is adjusted such that the amplifier output at the junction of R7, R8, is about 3.2V for all spans.
5. If the calibration board has to be replaced, adjust the cold junction compensation and the calibration as described.



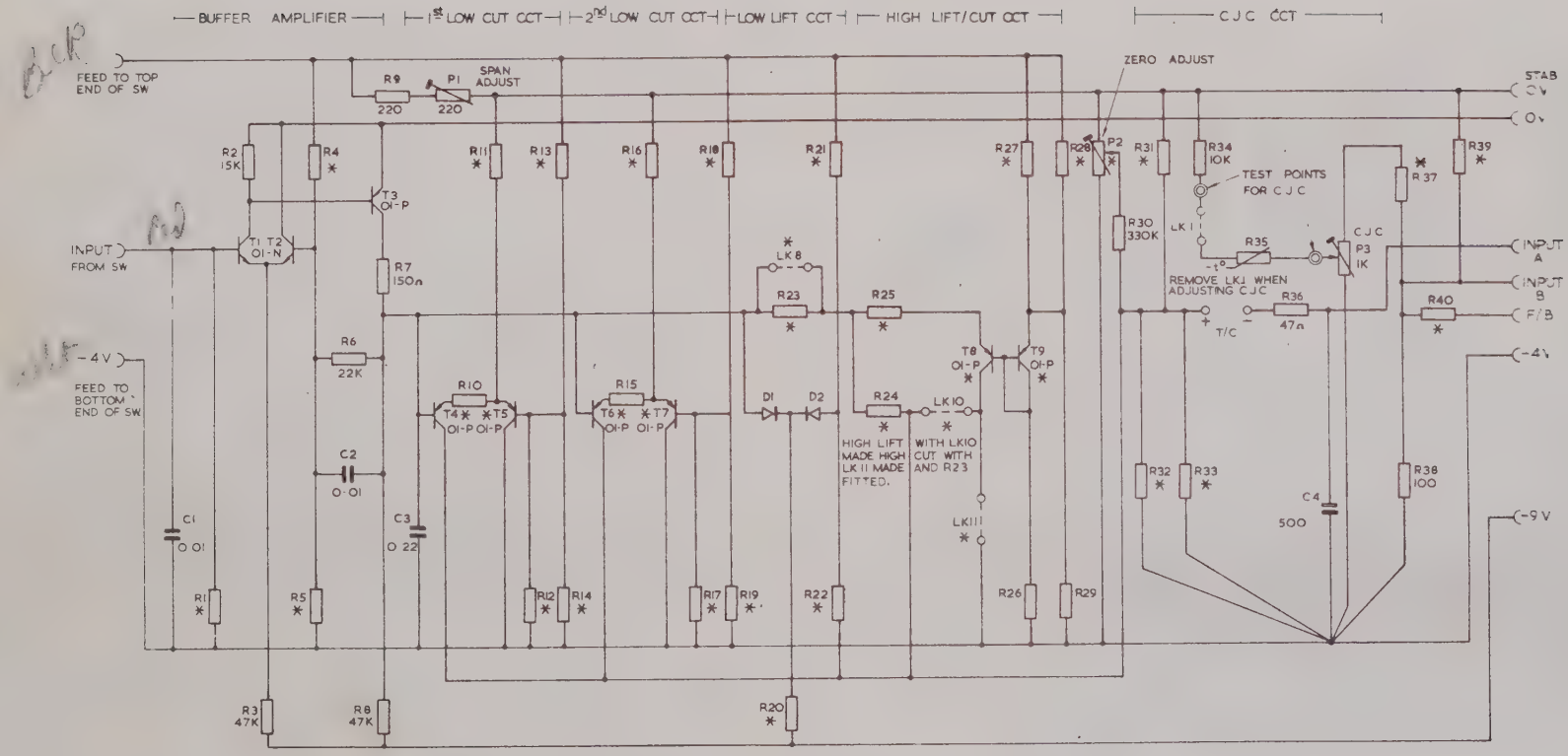
L.P. MkII DIGITAL T/C CAL Bd.

COMPONENTS SHOWN DOTTED ARE CAL. COMPONENTS.

R31 & R39 FIXED ZERO RESISTORS SELECTED ON TEST.

Drg No D93257

CIRCUIT No E92111 Sht 6


BUFFER AMPLIFIER
1st LOW CUT CCT
2nd LOW CUT CCT
LOW LIFT CCT
HIGH LIFT/CUT CCT
CJC CCT
FEED TO TOP END OF SW
SPAN ADJUST
ZERO ADJUST
STAB 0V
0V
INPUT FROM SW
FEED TO BOTTOM END OF SW
-4V
TEST POINTS FOR CJC
REMOVE LK1 WHEN ADJUSTING CJC
CJC P3 1K
INPUT A
INPUT B
F/B
T/C
-4V
-9V
HIGH LIFT MADE HIGH LK11 MADE FITTED.
WITH LK10 CUT WITH AND R23
R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40
C1 C2 C3 C4
T1 T2 T3 T4 T5 T6 T7 T8 T9
D1 D2
LK1 LK8 LK10 LK11
P1 P2 P3

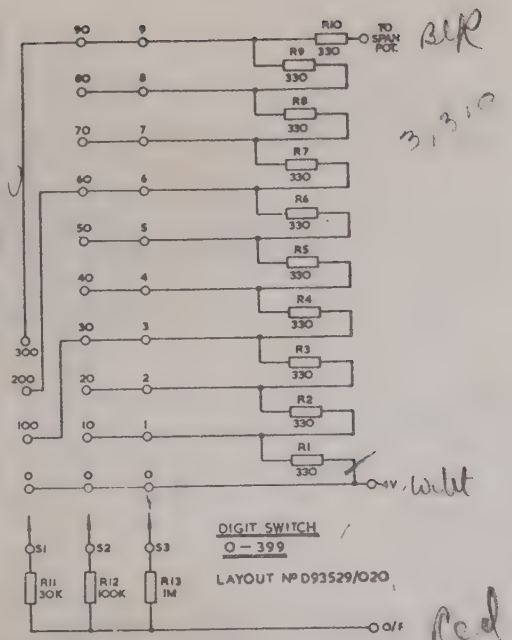
COMPONENTS SHOWN THUS * WILL BE OMITTED OR INCLUDED. & / OR THEIR VALUES WILL CHANGE, ACCORDING TO THE THERMOCOUPLE & SWITCH RANGE REFER TO WRITE UP FOR DETAILS

Drg No E92111 Sht 6

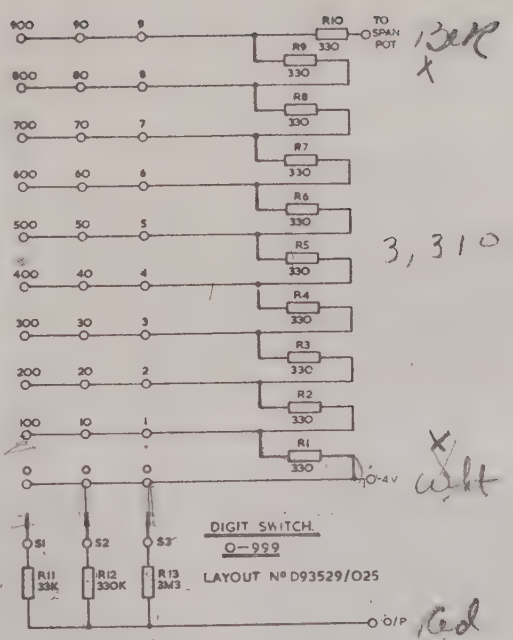
LILLIPUT MkII.

DIGITAL T/C CAL BOARD.

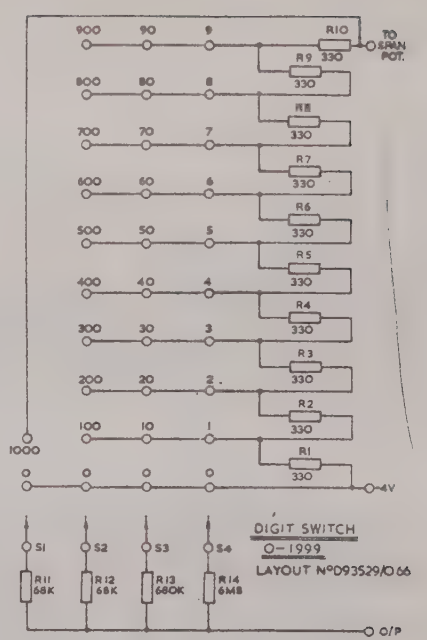
LAYOUT No D93257



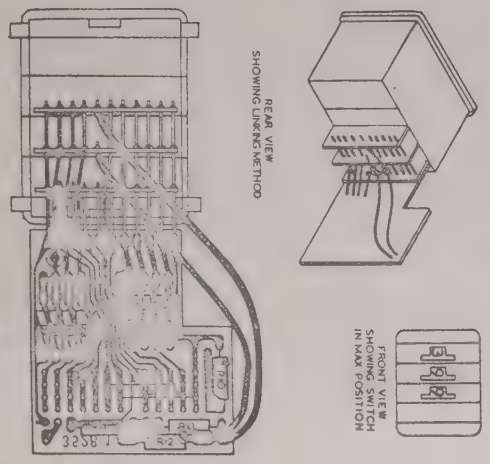
Drg Nº C92111 Sht 10



Drg Nº C92111 Sht 11.

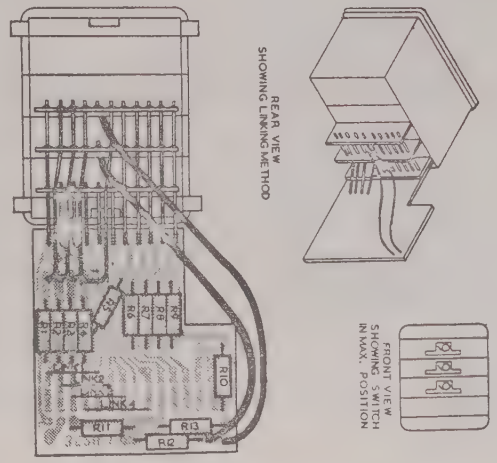


Drg Nº C92111 Sht 12



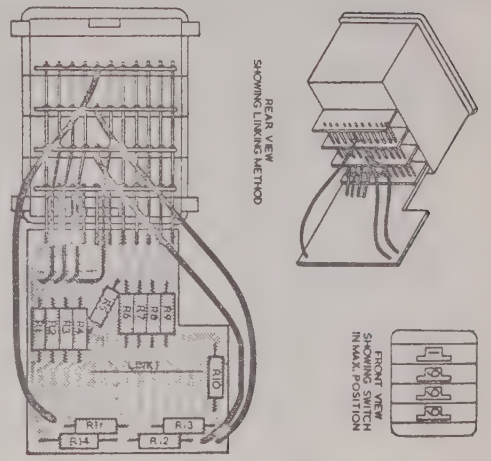
CIRCUIT Nº E92111 Sht 10.

Drg Nº D93529/020



CIRCUIT Nº E92111 Sht 11

Drg Nº D93529/025



CIRCUIT Nº E92111 Sht 12

Drg Nº D93529/066

Thermocouple digital calibration board.

The thermocouple digital calibration board subtracts the thermocouple emf from the digitally set reference voltage and feeds the resultant error signal into the main amplifier input.

Circuit Description

The reference voltage is obtained by the digital switches S1 to S3 (or S4). Linearisation is achieved by selection of resistors in the "hundred's" digit bank. The tens and units are obtained from this voltage by the potential divider R11 to R19, and the two summing resistors R9 and R10 on the calibration board. This method of linearisation allows for on the 0-999° range, for example 9 break points which means that the thermocouple curve may be very closely followed. This signal is then buffered, to prevent loading of the switch, by transistors, T1 to T4 and associated components. This buffered signal is then fed to R16 to provide the required reference voltage from which the thermocouple emf may be subtracted and this error signal passed to the main amplifier board. Cold junction compensation is provided by R19, R21, and P3. The negative temperature coefficient of the thermistor R24 in conjunction with the associated components will produce a voltage rise across R25 as the ambient temperature rises. The correct level of compensation being set by P3. Zero adjustment is provided by P2 and R18 and by resistors R11, R17 and R27 which vary with the range of instruments. Span adjustment is obtained by altering the current flowing through the switch resistor chain by R8 and P1. The network R20, C4 forms a series mode interference filter which rejects mains frequency pick up at the thermocouple input.

Checking.

1. Check all connections to the calibration board and measure thermocouple resistance, which should be less than 100 ohms.
2. With amplifier board plugged in and input connected to a mV source switch instrument on. Check voltage rails, stab. OV., -4V, -9V, -28V and OV.
3. The switch may be checked by placing a voltmeter between link 1 and checking for voltage changes when the digit setting is altered. The output of the buffer amplifier may be seen across resistor R16.

Calibration Procedure: (T/C Kelvin - Varley Board).

1. Place controller on level surface with mains switched off and set the meter mechanical zero by turning the nylon screw in the side of the meter.
2. Set Pot P1 on the mother board to minimum resistance (clockwise), connect a compensated mV source (see note below) with the correct compensating lead to the controlled, observing the polarity.
3. Switch on the mains and allow the instrument to warm up for 20 minutes.
4. Set the cold junction compensation in the following manner:-Turn the C.J.C. pot to -4V (clockwise when viewed from the top) ensuring the wiper is on the metal leg, short the thermistor and inject the C.J.C. mV according to the following table.

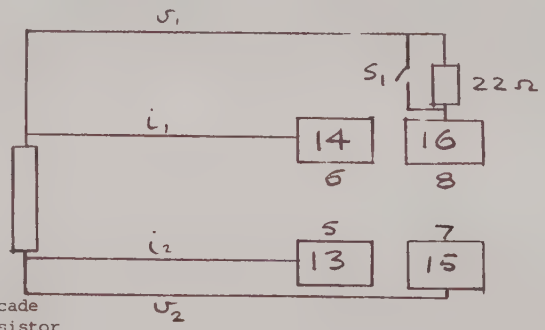
Thermocouple Type		C.J.C. mV
Iron/Con	J	5.56
Copper/Con	T	4.49
Chromel/Alumel	K	4.38
Pt.10%Rh/Pt	S	0.67
Pt.13%Rh/Pt	R	0.67

For any other thermocouple, mV = 5.35 (mV at 50°C - mV at 30°C).

Null the deviation meter by alteration of the digit switches and the zero Pot P2. Remove C.J.C. mV and renull the deviation meter with C.J.C. Pot P3. Remove thermistor short.

5. Set zero in the following manner, inject zero mV and with the digit switch set to zero, adjust the zero pot P2 to null the deviation meter.
6. Set span in the following manner:- Inject span mV and with the digit switch set the span, adjust the span Pot P1 to null the deviation meter.
7. Repeat 5 and 6 until no further adjustment is necessary.
8. Set the digit switch to the 70% of span position and inject mV to null the meter. Increase the digit switch setting by an amount which should give F.S.D. on the meter and adjust P1 on the mother board to give the correct meter deflection.
9. The thermocouple break protection may be checked by disconnecting one of the input leads and observing the indicator going upscale.

Note:- If the calibrator is an uncompensated potentiometer a cold junction correction must be made when setting the maximum and minimum signals on the potentiometer. The cold junction appears at the potentiometer terminals and a thermometer is usually located adjacent to these terminals for correction purposes. Read the temperature on this thermometer and obtain the equivalent millivolts from the thermocouple tables. Read the mV figures equivalent to maximum and minimum controller temperatures and subtract the cold junction mV from each of these figures. Use the corrected figure to calibrate the controller as above. If the minimum controller temperature is 0°C the subtraction gives a negative figure. Calibration at 0°C is achieved by reversing the polarity of the compensating lead at the potentiometer terminals and setting the potentiometer to the cold junction mV.

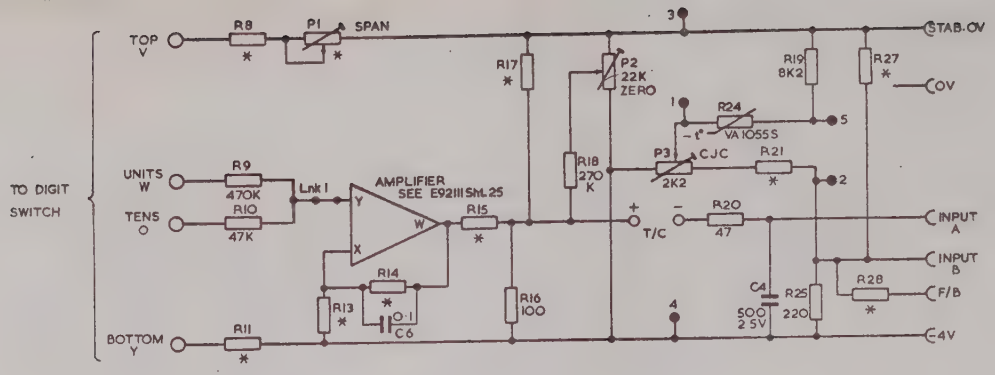


Terminal Nos.5,6,7 & 8 apply to models 020, 021.

Decade Resistor 0-999.9Ω ± 0.1%

Connections for Calibration of 017 or 018 with Pt RT Input.

THERMO-COUPLE	RANGE	CODE	P1	R8	R11	R13	R14	R15	R17	R21	R27	R28	COMP. CABLE
IRON – CONST B.S.	0–399°C	01272	1K	2K7	S.C.	47K	130K	12K	820K	18K		82K	C3221
			PTP102	RSY 272	LPB012	RTM473	RTM134	RTM123	RSY 824	RSY 183		RSY 823	
Ni/Cr – Ni/Al B.S.	0–399°C	03272	1K	2K7	S.C.	47K	130K	18K		22K		100K	C3222
			PTP 102	RSY 272	LPB 012	RTM473	RTM134	RTM183		RSY223		RSY 104	
COPPER CONST B.S.	0–399°C	04272	1K	2K7	S.C.	47K	100K	10K		18K		82K	C5343
			PTP 102	RSY 272	LPB012	RTM473	RTM 104	RTM 103		RSY 183		RSY823	
Pt / Pt 10% Rh. B.S.	200–1199°C	06169	1K	1K5	E33	100K	27K	22K		150K	1M5	150K	C3223
			PTP 102	RSY 152	RTD 033	RTM 104	RTM 273	RTM223		RSY 154	RSS 155	RTM154	
Pt / Pt 13% Rh. B.S.	200–1199°C	05169	1K	1K5	E 32	100K	27K	18K		150K	1M5	130K	C3223
			PTP 102	RSY 152	RTDO32	RTM 104	RTM 273	RTM 183		RSY 154	RSS 155	RTM134	
Ni/Cr Ni/Al B.S.	200–1199°C	03169	1K	1K5	E 34	470K	47K	4K7		22K		36K	C3222
			PTP 102	RSY 152	RTD 034	RTM 474	RTM 473	RTM 472		RSY 223		RTY 363	
Pt/Pt 10% Rh. B.S.	600–1599°C	06170	1K	1K2	E36	1M	27K	15K		150K	1M5	100K	C3223
			PTP 102	RSY 122	RTDO36	RTM 105	RTM 273	RTM 153		RSY 154	RSS 155	RTM 104	
Pt/Pt 13% Rh. B.S	600–1599°C	05170	1K	1K2	E35	1M	27K	13K		150K		91K	C3223
			PTP 102	RSY 122	RTD 035	RTM 105	RTM 273	RTM 133		RSY 154		RTY 913	
COPPER CONST B.S.	0–699°F	04281	470	1K2	S.C.	100K	100K	18K		18K	1M5	82K	C5343
			PTP 471	RSY 122	LPB012	RTM 104	RTM 104	RTM 183		RSY 183	RSS 155	RSY823	
Ni/Cr– Ni/Al B.S.	0–999°C	03276	1K	1K5	S.C.	470K	220K	6K8		22K		39K	C3222
			PTP 102	RSY 152	LPB 012	RTM 474	RTM 224	RTM 682		RSY 223		RSY 393	
Ni/Cr – Ni/Al B.S	0–999°F	03282	1K	1K5	S.C.	470K	82K	10K		22K	1M2	75K	C3222
			PTP 102	RSY 152	LPB 012	RTM 474	RTM823	RTM 103		RSY223	RSS 125	RTM753	
IRON – CONST B.S.	0–999°F	01282	1K	1K5	S.C.	100K	56K	10K		18K	1M2	56K	C3221
			PTP 102	RSY 152	LPB 012	RTM 104	RTM 563	RTM 103		RSY 183	RSS 125	RSY 563	
IRON-CONST. BS	200–1199°F	01283	1K	1K5	E40	470K	82K	6K8		18K	1M2	47K	C3221
			PTP 102	RSY 152	RTD 040	RTM 104	RTM 823	RTM 682		RSY 183	RSS 125	RTY 473	
IRON-CONST. BS	600–1599°F	01284	1K	1K5	E36	560K	130K	5K6	180K	18K		33K	C3221
			PTP 102	RSY 152	RTD 036	RTM 564	RTM 134	RTM 562	RTY 184	RSY 183		RTY 333	



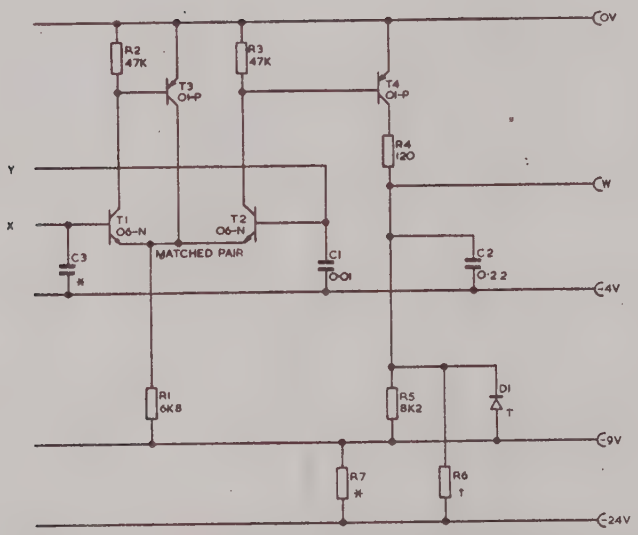
COMPONENTS MARKED THUS * DEPEND UPON RANGE & THERMOCOUPLE. SEE D4946 FOR VALUES.
—● DESIGNATES TEST POINTS (1-5) FOR CJC.

LP. Mk II. D.S.P. T/C CAL. BD.
LAYOUT No. E94830

9V

24V

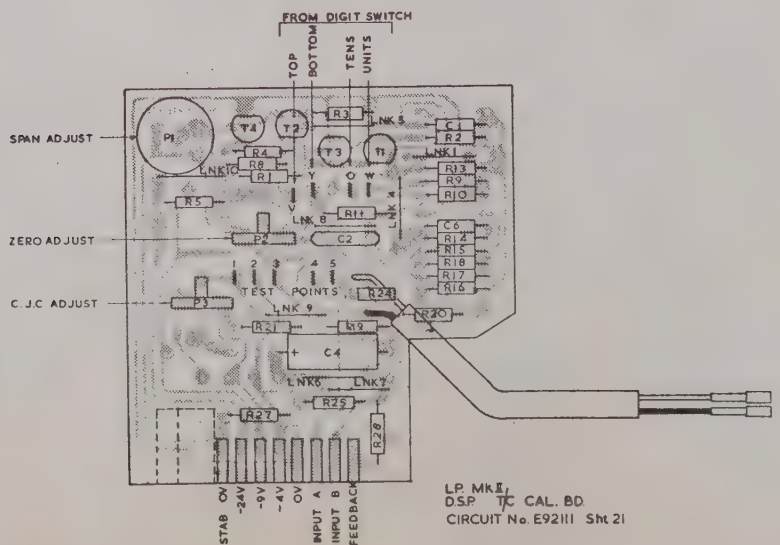
Drg. No. E92111 Sht 21



COMPONENTS MARKED * NORMALLY OMITTED.
COMPONENTS MARKED † MAY BE USED INSTEAD OF R5 FOR CERTAIN EXTERNAL SET POINT RANGES.

LP. Mk. II. AMPLIFIER FOR DIGITAL AND EXTERNAL SET POINT CAL. BD.
REFER TO E92111 SHTS 21,22,23,& 24.

Drg. No. E92111 Sht 25



LP. Mk II.
D.S.P. T/C CAL. BD.
CIRCUIT No. E92111 Sht 21

Drg. No E94830

DIGITAL (KELVIN - VARLEY) RESISTANCE THERMOMETER CALIBRATION BOARD.

The R/T calibration board subtracts the voltage developed across the R/T element from the digitally set reference voltage and the resultant error fed into the main amplifier input.

Circuit Description.

The set point circuit of the R/T calibration board is identical to that of the thermocouple type, the reference voltage being developed across R16. An almost constant current is passed through the R/T element by means of R22, P4 and R27, whose values are large enough that the lead resistance and change of the R/T element does not affect the current flowing through it. The voltage developed across the element is fed directly into input B via lead V2. The effect of lead V2 resistance is cancelled out by making the current in link V1 = 0 by the use of P4.
Calibration adjustment of zero and span is achieved by the use of P2 and P1 respectively.

Checking

1. With amplifier board plugged in and input connected to a decade resistance box switch instrument on. Check voltage rails stab 0V, -4V, -9V, -28V and 0V.
2. The switch may be checked by placing one lead of a voltmeter on link 1 and the other lead on -4V. Check for voltage changes when the digit setting is altered. The output of the buffer amplifier can be measured across R16.

Zero and Span Adjustments.

1. Place controller on level surface with supply switched off and set the meter mechanical zero.
2. Connect the input terminals to a resistance box as shown in the circuit below. Set P1 on the mother board to minimum resistance, (clockwise) switch on the supply and allow the instrument to warm up for 20 minutes.
The calibration points are at zero and at 80% of span, to minimuse the effect of slight gain change of the error amplifier with change of RT resistance.
3. Set resistance corresponding to low end of the range on the resistance box, and set the equivalent temperature on the digit switch. Adjust zero P2 on the calibration board to null the deviation meter. If the RT conforms to BS1904 or DIN 43760 the resistance/temperature table is found in Eurotherm publication TT2.
4. Set resistance corresponding to 80% of span on the resistance box, and the equivalent temperature on the digit switch. Adjust span pot P1 to null the deviation meter.
5. Repeat steps 3 and 4 until no further adjustment is necessary.

Deviation Meter Sensitivity Adjustment.

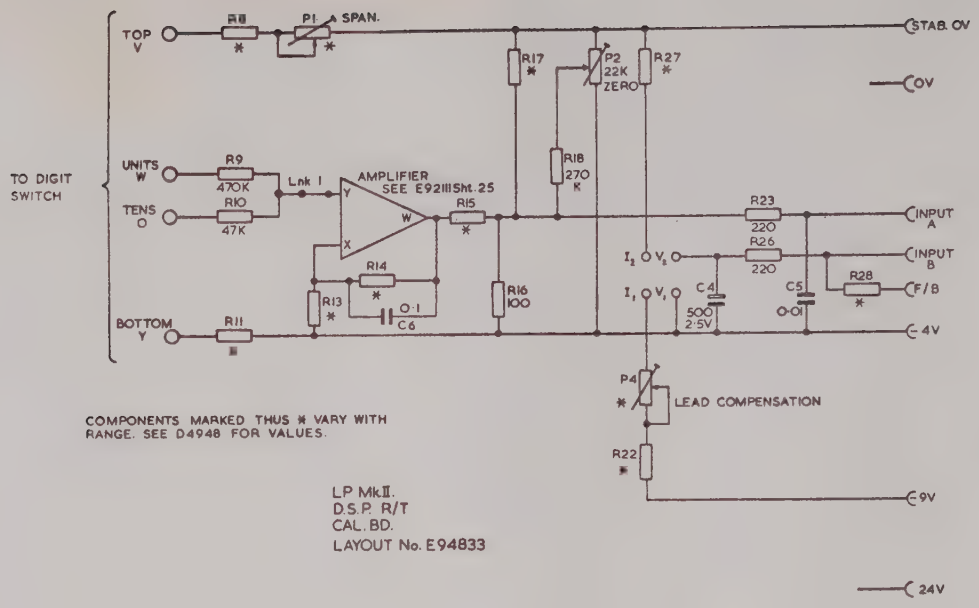
6. Set the decade box to a value equivalent to about 80% of span and set the digit switch to the same temperature. Chance the digit switch setting and adjust P1 on the mother board until the meter shows the same degrees change as the digit switch. (e.g. on a 0-99.9°C dial up to 85°C, with resistance for 80°C still switched in and adjust P1 for correct meter until the meter reads 5° downscale.

Lead Resistance Compensation Adjustment.

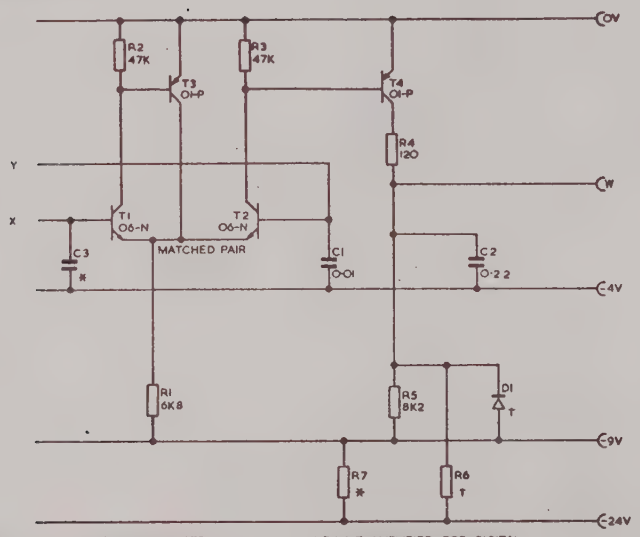
7. At 80% of span, remove shorting link S1, and adjust lead compensation Pot P4 until opening and closing S1 produces no change on the meter.

The pots may now be sealed to prevent movement by vibration.

ZERO RESISTANCE	RANGE	CODE	P1	R8	R11	R13	R14	R15	R17	R27	R28	P4	R22
100Ω	0-399°C	70272	1K	1K8	S.C.	56K	33K	10K	22K	22K	120K	10K	22K
			PTP 102	RSY 182	LPB 012	RTM 563	RTM 333	RTM 103	RSY 223	RTM 223	RSY 124	PMV 103	RTM 223
100Ω	0-999°C	70276	1K	2K2	S.C.	56K	33K	10K	62K	56K	220K	25K	56K
			PTP 102	RSY 222	LPB 012	RTM 563	RTM 333	RTM 103	RSY 623	RTM 563	RSY 224	PMV 253	RTM 563
93.933Ω	0-999°F	70282	1K	2K2	S.C.	120K	47K	6K8	27K	24K	120K	10K	24K
			PTP 102	RSY 222	LPB 012	RTM 124	RTM 473	RTM 682	RSY 273	RTM 243	RSY 124	PMV 103	RTM 243
100Ω	0-199°C	70271	1K	1K5	S.C.	47K	82K	10K	12K	12K	130K	4K7	12K
			PTP 102	RSY 152	LPB 012	RTM 473	RTM 823	RTM 823	RSY 123	RTM 123	RTM 133	PMV 472	RTM 123
100Ω	0-99.9°C	70270	1K	2K2	S.C.	82K	39K	10K	6K2	6K2//820K	120K	2K2	6K8
			PTP 102	RSY 222	LPB 012	RTM 823	RTM 393	RTM 103	RSY 622	RTM 622 RSY 824	RSY 124	PMV 222	RTM 682



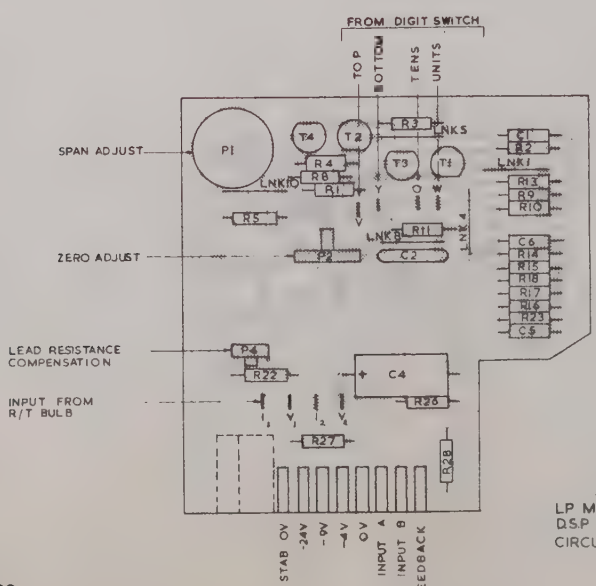
Drg. No. E92111 Sht. 22



COMPONENTS MARKED * NORMALLY OMITTED.
COMPONENTS MARKED † MAY BE USED INSTEAD OF R5 FOR CERTAIN EXTERNAL SET POINT RANGES.

LP Mk.II AMPLIFIER FOR DIGITAL AND EXTERNAL SET POINT CAL BD. REFER TO E9211I SHTS 21,22,23,& 24.

Drg. No. E92111 Sht 25



LP MK II,
D.S.P. R/T CAL BD
CIRCUIT No E92111 Sht.22

Drg. No. E94833

MAIN AMPLIFIER BOARD

Function

The main amplifier board converts a microvolt level error signal in the range 0 to one proportional band from the calibration board into a 0 to 4.4V signal suitable for driving the output stage. The output signal varies between the -4V and -9V levels, corresponding respectively to minimum and somewhat greater than maximum output from the controller. It is convenient to see the -4V line as reference for signal purposes.

Circuit Description

The board consists of three main sections, an error amplifier, a three-term amplifier and part of the stabilised power supply. The error amplifier is a temperature stabilised high-gain non inverting d.c. amplifier with a gain control in the feedback network which allows the gain, and hence the proportional band, to be varied over a 5:1 range. The error amplifier drives the three-term amplifier. The three term amplifier introduces integral and derivative action into the control loop to enable accurate control at the desired temperature with no offset. The proportional band of the controller is defined as the change in input signal required to produce a change in output signal from zero to 100%. The controller prop. band thus corresponds to an output signal change of 4.4V at the three term amplifier output. The three term amplifier has a gain of 5.5 for the standard model with a 2% to 10% proportional band. The controller proportional band thus corresponds to an error amplifier output of 0.8 volt.The minimum gain of the error amplifier is set to produce an output of 0.8 volt when an error signal of 10% of span is applied at the input. Alternative models have a proportional band variable 1% to 5% of span or 5% to 25% of span achieved respectively by increasing the three term amplifier gain to 11 or decreasing the three term amplifier gain to 3. A desaturation network placed across the three term amplifier prevents amplifier saturation and enables derivative action to take effect some distance away from the set-point thereby minimising overshoot and reducing settling time from warm-up. The output control signal is fed to the output board via a maximum power control. The power supply section provides a temperature stabilised 0 to -4V supply for the amplifier circuit and 0V stabilised to -4V supply for the calibration board. This latter supply differs only by the pd across R31 whose purpose is to give slope resistance compensation for the incremental resistance of T13.

Error amplifier

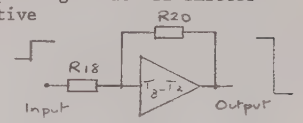
Transistors T1 to T5 and associated components form a high-gain low-drift d.c. amplifier with overall positive gain from T1 base to T5 collector. Input transistors T1, T2 are a matched pair connected differentially and surrounded by a heat sink to give very low temperature drift. Potentiometer P2 is included to balance out any difference in the resistance values of R5, R6 and set up the amplifier to give a 0V output with no input signal applied. The differential signal at the collectors of T1,T2 is further amplified by the differentially connected transistors T3, T4 and a single-ended output is provided at the collector of T5. The overall gain of the amplifier is set by providing negative feedback from T5 collector to T2 base via P1, R3 and calibration board resistors R6, R9. Potentiometer P1 is included in the feedback network to vary the proportional band over a 5:1 range by varying the gain of the amplifier. Different proportional band ranges of 1% to 5% of span, 2% to 10% of span or 5% to 25% of span are achieved by fixing the three term amplifier gain at 11, 5.5 or 3 respectively. The proportional band of the controller thus corresponds to an error amplifier output of 0.4 volt on the model with a 1% to 5% proportional band, 0.8 volt on the model with a 2% to 10% proportional band, or 2 volts on the model with a 5% to 25% proportional band. With the proportional band potentiometer P1 set to its maximum position, the gain of the error amplifier is set to give an output signal of 0.8V, with respect to the -4V line, when an input error signal of 10% span is applied to T1 base. When P1 is set to its maximum position the error amplifier gain is defined by (R9 + R6)/R6, these resistors being situated on the calibration board. The error amplifier output is measured at the junction of R12, R13 (equals pin d1 on the derivative link). Diode D1 limits the amplifier output to approximately -6V. Network R8, C4 provides rejection of 50 or 60Hz series mode interference by reducing the a.c. gain of the error amplifier. Isolation of the whole circuit gives common mode rejection enabling the thermocouple to be elevated 240V a.c. above ground if necessary. Capacitors C4a and C4b are connected in series in opposite polarity to accommodate voltages of either polarity, with reference to -4V, at the amplifier output. Network C3, R7 provides amplifier stabilisation and capacitors C1, C2, C5 provide interference rejection.

Three term amplifier

The three term amplifier T8 to T12 has a high input impedance FET T8 as the input stage to make it suitable for use with the high value resistors R18, R20 required for the derivative and integral action. The amplifier has overall negative gain from T8 base to T12 emitter, the gain being defined approximately by the ratio R20/R18 and set to a value 10, 5 or 2 respectively for proportional band ranges of 1% to 5%, 2% to 10% or 5% to 25%. A -4V input to T8 from the error amplifier results in a potential of approximately 1 volt across R22 due to the current through T8. This voltage is balanced out at T10 base by potentiometer P6 to set up the correct bias condition of 0V at T12 emitter when a 0V input is applied to T8 base. Capacitors C6 and C8 provide derivative and integral action respectively and capacitors C9, C10 provide interference rejection.

Proportional action

Proportional-only action can be achieved by opening link d1-d2 to remove derivative action and making link I1 - I2 to remove integral action. In this condition T12 acts as an emitter follower and the output signal at T12 emitter follows the signal at the junction of R27, R28. Negative feedback is applied via R20 and the gain of the three term amplifier is defined by R20/R18. The three term amplifier has a gain of 4.5 for controllers having a 2% to 10% proportional band. A 0.8 volt input change from 0 to +0.8V, corresponding to a temperature change from set point to one proportional band below set-point, thus produces a 4.5 volt output and causes the output power to increase from zero to 100%. For controllers having a 1% to 5% proportional band the three term amplifier has a gain of 10; an input change from 0 to 0.4V producing an output change from 0 to 4.5V.. For controllers having a 5% to 25% proportional band the three term amplifier has a gain of 2; an input change from 0 to 2V producing an output change from 0 to 4V. The output voltage at T12 emitter is prevented from becoming more negative than the collector voltage by emitter-follower action. Potentiometer P4 thus acts as a maximum power limit by restricting the negative excursion at T12 emitter. Diode D4 protects R12 from excessive reverse voltage when P4 is set to its minimum position.

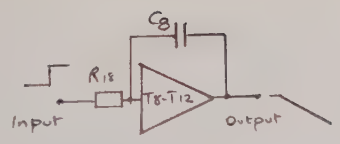


Proportional Action

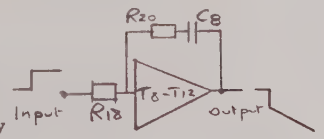
Integral action

Integral action is achieved by placing capacitor C8 in series with the feedback resistor R20. The gate of T8 is held at 0V by normal amplifier action and the

current through R21 is negligible due to the very high input impedance of FET T8. When the error amplifier output is positive with respect to the -4V line corresponding to under temperature, a current flows through R18 due to the potential difference across R18. The three term amplifier output goes negative with respect to the -4V line such that all of the input current in R18 flows through R20. The negative movement at the amplifier output causes the output power to increase in proportion to the error. The input current through R18 and R20 causes capacitor C8 to charge in a direction which produces in addition a negative ramp at the amplifier output, the amplifier output automatically adjusting to balance the currents in R18 and R20. The negative ramp at the amplifier output causes a further gradual increase in output power. As the output power increases the temperature rises and the input signal reduces. When the load temperature achieves the desired temperature the input signal (being the difference) falls to 0 and the capacitor ceases to charge. In practice C8 will always acquire just sufficient charge to enable the required output power to be maintained with a 0V signal representing zero error from the error amplifier.



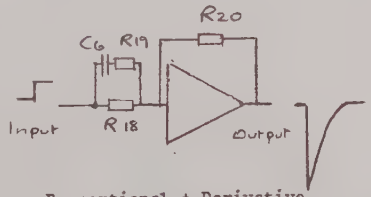
Integral Action



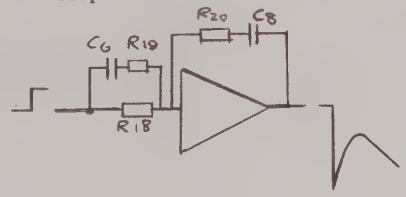
Proportional + Integral Action

Derivative action

Derivative action is achieved by placing network C6, R19 across the input resistor R18. When the temperature is changing the derivative capacitor C6 presents a low impedance which shunts R18 and increases the amplifier gain. With rapid input changes the capacitor C6 presents a short circuit and the amplifier gain is increased from $\frac{R20}{R18}$ to approximately $\frac{R20}{R19}$, assuming R19 has a much lower resistance than R18. The amplifier gain increases as the rate of change of temperature increases and the corresponding rapid change of output power acts in a direction which will reduce the rate of change of temperature. When the temperature is steady the derivative action dies away as C6 recharges through R18, R19. During warm-up when the temperature is a long way below set-point, T5 collector limits at 4V and causes C6 to charge by 4 volts. When the temperature reaches a point 40% of span below set point T5 collector starts to move negatively and the change is transmitted immediately to the three term amplifier by the charge on C6, giving normal derivative action 40% of span below set-point, provided the proportional band is set to maximum, and reducing the output power in proportion to the rate of rise of temperature. Derivative action will start to take effect 8% of span below set-point if the proportional band is set to minimum. Capacitor C8 also charges whilst T5 collector limits at 4V and is equivalent to moving the proportional band upscale. Discharge of the derivative capacitor C6, as the temperature rises, allows partial discharge of the integral capacitor C8, moving the proportional band downwards from its upscale position. This effect, combined with the derivative action, minimises temperature overshoot. The relative values of C6 and C8 are chosen to minimise overshoot without increasing warm-up time.



Proportional + Derivative



Proportional + Integral & Derivative

Desaturation network

Operation of normal derivative action outside the proportional band, as described above, is dependent on virtual-earth (OV)) condition being maintained at the input to the three-term amplifier, since a saturated amplifier would be unable to act on the signal transmitted by C6. Transistors T6, T7 and associated components maintain a virtual-earth at the three-term amplifier input by switching additional feedback if the amplifier approaches saturation. The base of T7 is held at -5V. If T11 collector falls to -6V transistor T7 conducts and reduces the amplifier input by producing a voltage across R17. The base of T6 is held at +2V by potential divider R15, R16. If T11 collector rises to +3V transistor T6 conducts and reduces the amplifier input by producing a voltage across R17. Diodes D2 and D3 protect transistors T6 and T7 respectively from reverse voltage.

Power Supply

A reference voltage of -8.2V is provided across Z1 by the current through the mother-board resistor R11. Potential divider R33, R34 across Z1 provides a reference voltage of -3.3V at T13 base. Transistor T13 across as an emitter-follower and provides a stabilised -4V supply at the emitter. The values of R33, R34 are chosen such that the negative temperature coefficient of T13 base-emitter junction compensates for the positive temperature coefficient of Z1, providing a temperature compensated -4V supply for the set point calibration board. Mains voltage compensation has to be provided for the stabilised -4V set-point supply, since a fall in mains voltage reduces the current through mother-board resistor R11 and causes a slight fall in the reference voltage across Z1 due to its slope resistance. Compensation is achieved by resistor R31 on the amplifier board and resistor R9 on the mother-board. A fall in mains voltage produces a fall in current through R9. This reduces the voltage drop across R31 which compensates for the slight change of the -4V supply.

Integral and Derivative Times

With proportional-only action the gain of the three term amplifier is equal to the ratio $\frac{R20}{R18}$ and this gain determines the proportional band of the controller. The standard 2% to 10% proportional band is obtained with a three term amplifier gain of 4.5. Alternative 1% to 5% or 5% to 25% proportional band ranges are obtained with gains of 10 or 2 respectively. With proportional plus derivative action the derivative time is equal to R18, C6 seconds. With proportional plus integral action the integral time is equal to R20.C8 seconds. With three term, proportional plus derivative plus integral, action the amplifier gain and time constants alter slightly and are calculated as follows.

Integral Time TI = T1 + T2 where T1 = R18.C6 & T2 = R20.C8

Derivative time $TD = \frac{T1.T2}{T1+T2}$ Amplifier gain $K = \frac{R20}{R18} + \frac{C6}{C8}$

The transfer function of the amplifier is

$K(1 + \frac{1}{TI}\int dt + TDd\frac{}{dt})$ or $K(1 + \frac{1}{STI} + STD)$ S=Laplace operator

The standard values T1 and T2 are 70 seconds and 330 seconds respectively, giving derivative and integral times of 60 seconds and 400 seconds respectively. The capacitors C6 and C8 are usually of equal value in order to provide an adequate amount of overshoot suppression, the amount of suppression increasing as the value of C6 is increased. The following tables show resistor and capacitor values required for various values of T1 and T2 with different proportional bands. Note that T1 predominates in the derivative time and T2 predominates in the integral time.

PROP. BAND 1% to 5%
R18=15MΩ R20=150MΩ

T1 Sec	C6 µF	T2 Sec	C8 µF	TD Sec	TI Sec
3	0.22	33	0.22	2.8	36
7	0.47	70	0.47	6.3	77
15	1.0	150	1.0	14	165
33	2.2	330	2.2	28	360
50	3.3	500	3.3	45	550
70	4.7	700	4.7	63	770
100	6.8	1000	6.8	90	1100

PROP. BAND 2% to 10%
R18=33MΩ R20=150MΩ

T1 Sec	C6 µF	T2 Sec	C8 µF	TD Sec	TI Sec
7	0.22	33	0.22	6	40
16	0.47	70	0.47	13	86
33	1.0	150	1.0	30	163
70	2.2	330	2.2	60	400
110	3.3	500	3.3	90	610
160	4.7	700	4.7	130	860
220	6.8	1000	6.8	180	1220

PROP. BAND 5% to 25%
R18=75MΩ R20=150MΩ

T1 Sec	C6 µF	T2 Sec	C8 µF	TD Sec	TI Sec
16	0.22	33	0.22	11	49
35	0.47	70	0.47	23	105
75	1.0	150	1.0	50	225
160	2.2	330	2.2	108	490
250	3.3	500	3.3	167	750
350	4.7	700	4.7	230	1050
500	6.8	1000	6.8	330	1500

Control System Optimisation

Standard PI and D Settings

The 2-10% proportional band, 60 sec TD and 400 sec TI normally supplied have been selected to give stable control over a wide range of industrial applications. It is usual to operate with the smallest setting of the proportional band possible without oscillation of the control loop. If oscillation persists at the maximum setting the next higher proportional band range may be chosen.

Non Standard P, I and D Settings

If control is either too oscillatory or too loose convert the controller to P only by opening link d1, d2 and closing link I1, I2. The temperature will settle downscale due to the absence of integral action.

If oscillation occurs at maximum proportional band the system gain is too high. An excessive heater rating or an oversized valve are typical causes.

When stable control has been obtained slowly reduce the proportional band until the system just begins to oscillate with period T at proportional band say X. Depending on how lively or sluggish the process is, one may need to wait anything from 1 minute to 20 minutes between adjustments to see if oscillation will occur.

Select the nearest tabulated values of C6 and C8 which give TI=T/2. The value of TD follows automatically from the table. Increase the proportional band to 1.7X. Because processes differ further adjustments may give better results Smaller values of TI and TD give tight control with a tendency to oscillate. Larger values give more stable control and longer recovery time from disturbances.

Amplifier Checking and Adjustment

A simple first in situ check is to dial a set point well above indicated temperature, turn the power limit adjustment to maximum and note that full power output is obtained; next move the set point gradually downwards well below indicated temperature and note that the power output falls to zero.

Power Supply Checks

Ensure that the amplifier and calibration boards are plugged in to the mother board. Relative to the OV line check the -4V, -9V, -28V lines and point X (-8.2V). The OV and OV stab lines differ only by some 20mV.

The amplifier is more accessible if it is plugged in via the extension board part No.E3917A.

Signal Range checks and Zero Adjustments

✳(All measurements are taken with respect to the -4V line with Link I1, I2 - closed and d1, d2 open).

Error Amplifier

To check gain

Turn P1 (proportional band) to maximum and apply an input signal from the millivolt source which is 10% of instrument span below set point. The voltage at d1 should be +0.8V. At minimum setting of P1 an input 2% below set point should give +0.8V at d1. With RT instrument do this check with an input signal of 80% span because gain is dependent on the RT resistance. The dynamic range of this signal is about +3.7V to about -5.7V corresponding to large downscale and upscale deviations respectively.

To adjust zero

The amplifier zero is set by P2 at the factory. It is only necessary to readjust if P2 has been disturbed or if R5, R6, P2 or the matched pair T1, T2 have been changed. To adjust, connect input A and input B to the -4V line and adjust P2 until the deviation meter of the instrument goes through null. This adjustment is very sensitive because of the high gain without feedback of the error amplifier, therefore it is not possible or necessary to achieve exact null.

3 Term Amplifier.

To check gain

Turn proportional band and power limit to maximum, ensure that link d1, d2 is open and I1, I2 closed. Connect a dc voltmeter to measure the control signal at the output of the 3 term amplifier (I1 to -4V line). Dial a set point 5% of span above indicated temperature (for RT instrument make indicated temperature 80% of span). This puts +0.4V into the 3 term amplifier. The voltmeter should now show this signal amplified by a factor $-\frac{R20}{R18}$ which is -2. -4.5 or -10 for respectively 5-25%, 2-10% or 1-5% proportional bands. For large deviations above and below set point the control signal should swing to respectively -5V and +3.7V. Some output boards have a diode which limits the + swing to about 0.7V.

To check power limit.

With temperature well below set point ensure that the -5V output (I1 to -4V line) can be turned down to 0 when power limit is fully anti-clockwise.

To check Zero.

With proportional band at maximum adjust the set point until the voltage at d1 (or error signal pin on alarm board position) is zero. The control signal (at I2 or control signal pin on the amplifier board) should now be zero. If not, reset the 3 Term amplifier as follows:- Remove the d1/d2 link and make the I1/I2 link. Short circuit the junction of R17 and R18 to the -4V rail. Connect a voltmeter between the I1/I2 link and the -4V rail. Adjust P3 until the 3 Term Amplifier output is zero. Remove the shorting link. It is convenient now to check that the temperature deviation meter is no more than 0.5mm from zero. If not, change the matched pair T1, T2 on the mother board provided that the mechanical zero of the meter is correct.

Make link d1/d2 and open link I1/I2 to restore derivative and integral action. If control offset is still present when the controller is in use this could be due to faulty or leaky capacitors C6 or C8. Offset may also occur in systems where the cycle time of the instrument output is long compared with the response time of load and sensor. A solution is the reduction or removal of C6.

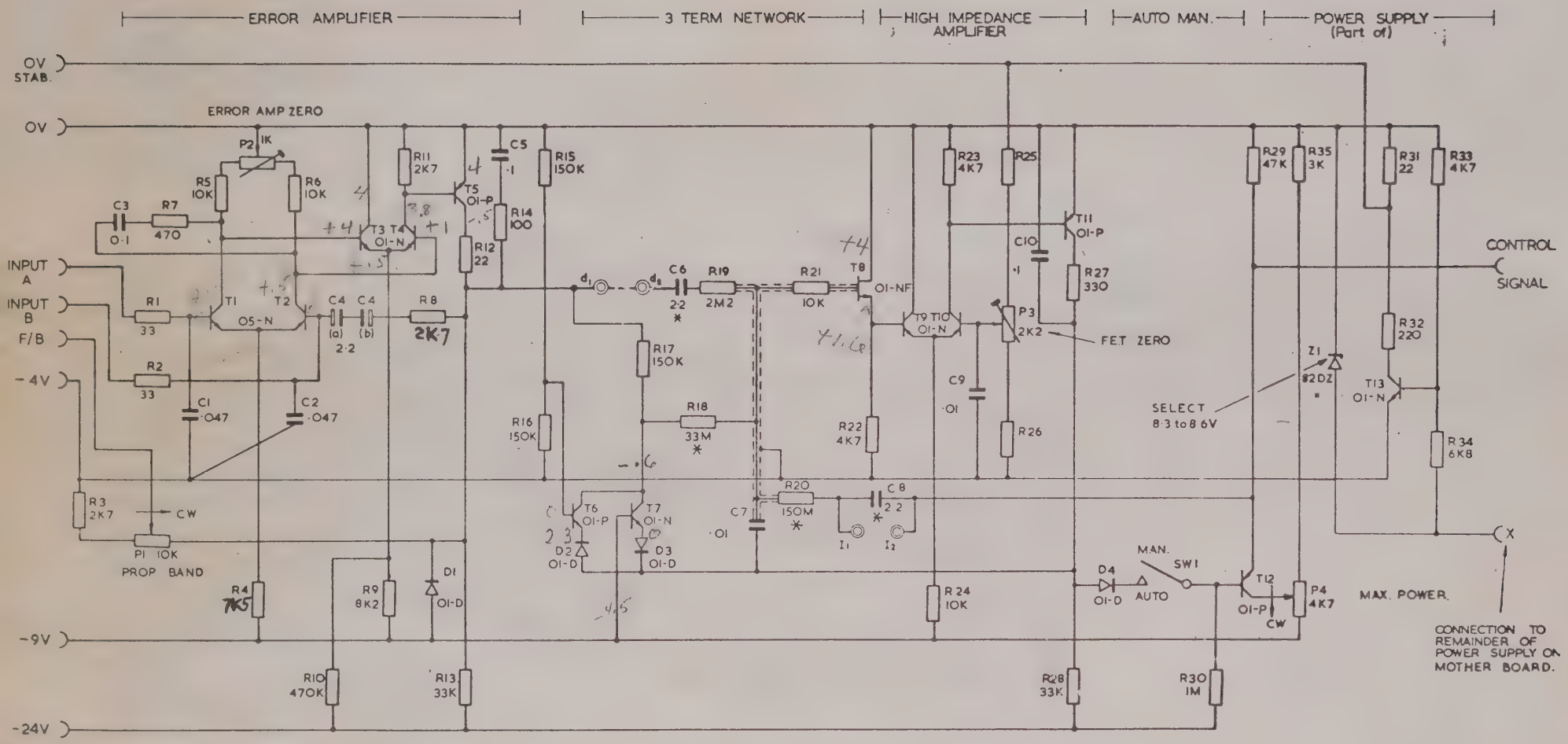
Voltage Table

Typical dc test voltages for all the transistors are shown in the table, measured with a 20KΩ/volt 10v meter. Test conditions are d1, d2 open, link I1, I2 closed, power limit control fully clockwise, output board and calibration board removed, input A or B connected to the -4V line.
All measurements are with respect to the -4V line.

X. cannot be measured by 20KΩ/V meter because of high source impedance.

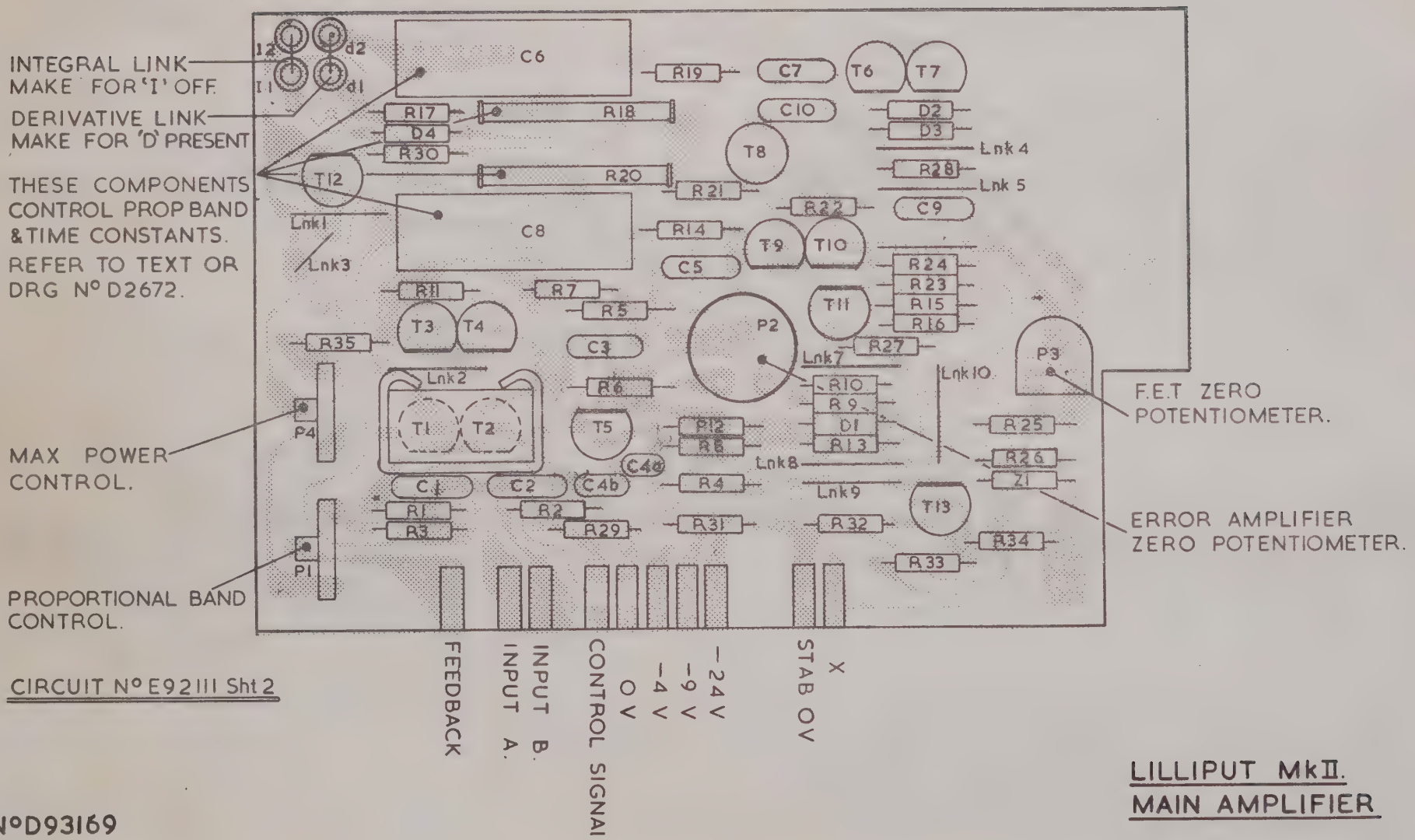
		T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	
Which input connected to -4V line.	A	-0.5	-0.5	+3.2	+3.2	+4	+2.5	-5.3	+1.2	+0.7	+0.7	+4	-4.7	0	Emitter
	B	-0.5	-0.5	+3.4	+3.2	+4	+2.5	+4.3	+1.2	+0.7	+0.7	+4	+3	0	
	A	0	0	-0.5	+4	+3.3	+2.5	-4.7	X	+1.2	+1.2	+3.4	X	+0.7	Base
	B	0	0	+4	-0.5	+4	+2.5	-4.7	X	+1.2	+1.2	+3.4	X	+0.7	
	A	-0.5	+4	+4	+3.3	+4	+1	+1	+4	+4	+3.4	-5.6	-4.7	+3	Collector
	B	+4	-0.5	+4	+4	-5.3	-0.5	-0.5	+4	+4	+3.4	+3.4	-4.7	+2.8	

Drg N° E92111 Sht 2.



COMPONENTS MARKED THUS * VARY WITH MODE OF OPERATION.
REFER TO WRITE UP FOR DETAILS.
R25 & R26 ARE DEPENDENT UPON F.E.T. SEE DR'G N°C 4367
LAYOUT N° D93169

LILLIPUT Mk II.
MAIN AMPLIFIER.



CIRCUIT Nº E92111 Sht 2

LILLIPUT MkII.
MAIN AMPLIFIER

Drg NºD93169

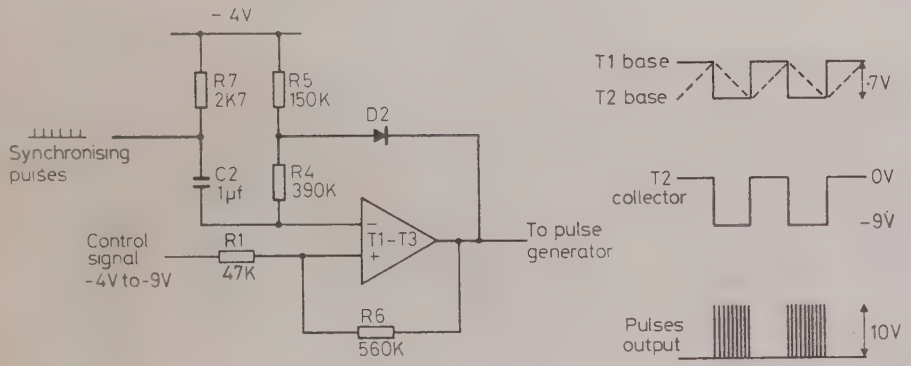
FAST CYCLE PULSE OUTPUT BOARD. (001)

Function

The fast cycle pulse output board converts a 0 to 5V d.c. input signal into trigger pulses suitable for driving thyristors.

Circuit Description

The input control signal operates between the levels -4V and -8.2V corresponding respectively to minimum and maximum output power. The output pulses are generated on a time proportioning basis with an ON + OFF period of approximately 120 + 120 Sec at half power. The commencement of trigger pulses is synchronised to the zero voltage crossover point of the mains cycle to minimise interference. Power feedback is employed so that the load power remains constant if the mains voltage varies.



Transistors T1 to T3 and associated components form a high-gain d.c. amplifier with overall positive gain from T1 base to T3 collector and positive feedback via R6. With an input control signal of -7V transistors T1 and T3 switch off and the collector of T3 falls to a potential of approximately -9V as defined by resistors R9, R10. Positive feedback via R6 causes the potential at T1 base to fall to -7.2V. Diode D2 conducts causing capacitor C2 to charge negatively towards -9V (T3 collector potential) via R4. When C2 has charged to -7.2V, transistors T1 and T3 conduct and T3 collector potential rises to 0V. Positive feedback via R6 causes T1 base potential to rise to -6.5V ensuring that T1 and T3 remain hard on. Diode D2 is reverse biased and C2 commences to discharge towards -4V via R4, R5, R7. Capacitor C2 discharges to -6.5V after approximately 120m Sec, at which point transistors T1 and T3 switch off the positive feedback via R6causes T1 base potential to fall again to -7.2V and capacitor C2 charges negatively from -6.5 towards -9V (T3 collector potential) via R4, D2. Capacitor C2 charges to -7.2V after approximately 120m Sec at which point T1 and T3 conduct and the cycle is repeated. With an input control signal of -7V capacitor C2 thus charges and discharges continually between the levels -6.5V and -7.2V, producing a square wave of period approximatley 120 + 120m Sec and magnitude approximately 9 volts at T3 collector. The output oscillator switches ON whenever T3 collector is negative. The ON - OFF switching differential of 0.7V at T1 base remains approximately constant as the input control signal varies, but the switching level follows the control signal. As the input control signal becomes more negative the average level of charge on C2 becomes more negative, causing the charging current via D2 to decrease and the discharge current to increase. This gives an increasing output OFF time until the output oscillator stays permanently ON when the control signal becomes more negative than T3 collector potential (approximately -9V). As the input control signal becomes less negative the output ON time decreases and the OFF time increases until the output oscillator stays permanently OFF with an input control signal of less than -4V.

Synchronisation.

The commencement of the ON period of the output pulses is synchronised to the zero voltage crossover point of the mains cycle by components R7, R8, D1, D3. The negative full-wave-rectified unsmoothed waveform at D3 cathode produces a positive pulse of approximately 0.2V magnitude across R7 at each crossover point in the mains cycle due to the conduction of D1 when the waveform falls to zero. The positive pulse is transmitted to T2 base via C2 and this synchronises the commencement of output pulses to the crossover point in the mains cycle. The controller and load supplies must be from the same phase of the mains supply for the synchronisation to be effective.

Power Feedback.

Due to the square law relationship between voltage and power, a 10% rise in mains voltage will produce a 20% rise in load power unless the output ON time reduces to compensate for the change. A 10% rise in mains voltage causes a 10% rise in the smooth, but unstabilised, -28V supply. This produces a 10% change in T3 collector voltage from -9V to -9.9V during the period when the output oscillator is ON. The increased charging current through R4, D2 reduces the output ON time by approximately 20% and this compensates for the change in supply voltage.

Pulse Generator.

The blocking oscillator formed by T4, TX1 and associated components provides thyristor trigger pulses at the output windings whenever T3 collector potential falls to -9V. The pulses have an amplitude of 10 volts, a duration of 12/uSec and a repetition rate of four pulses per millisecond. When T3 collector falls to -9V transistor T4 is biased into conduction by the base current through D4, R11 and R12. The voltage appearing across the primary winding of TX1 reflects an additional bias voltage across C6, R13, in such direction that the conduction of T4 is increased. The regenerative action of C6, R13 causes the conduction of T4 to increase to saturation, applying 28V across the primary of the transformer and producing a bias voltage of 6 volts and an output of 10 volts as defined by the turns ratio of the transformer. Capacitor C6 charges via T4 base and R13 after approximately 12/uSec and T4 then begins to switch off. The voltage across the transformer primary starts to reduce and the regenerative action of the bias winding causes T4 to switch off rapidly due to the charge on C6. When conduction in T4 ceases the inductance of the transformer causes the primary voltage to reverse. D5 and R14 and C5 provide a

path for the magnetising current to protect T4 from excessive voltage and controls the size of the overswing of the negative pulse at the output. Capacitor C6 discharges via R11, R12, R13, until T4 is again biased into conduction after approximately 250/uSec, generating a further 12/uSec pulse at the output. The action continues until T3 collector potential rises to 0V. Capacitor C3 prevents the pulses from reaching T3 collector and C4 prevents spurious triggering of the oscillator due to noise.

Calibration Procedure.

1. Demand maximum output from the 3 Term amplifier with link I1, I2 made and d1, d2 open circuit. Attach a voltmeter between link I1, I2 and -4V and adjust the power pot P4 on the amplifier board to give a zero reading on the meter. Adjust P1, on the output board to give zero output.
2. Demand maximum power from the 3 Term amplifier and increase the mains supply by 10%, adjust the span pot P2 to give maximum power out.

Checking.

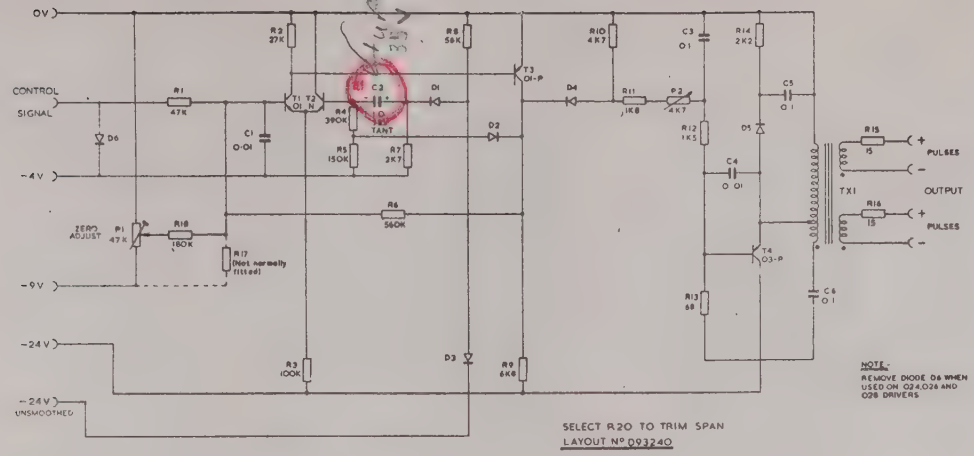
1. With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -4V, -9V, -24V, and -28V supplies with a d.c. voltmeter. Failure of any of the supplies could be due to a mother board or amplifier board fault.
2. Connect a 10V d.c. voltmeter between the control input and 0V terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.
3. Set the input control signal to -6.5V and monitor one output winding with an oscilloscope. Bursts of pulses, of magnitude 10 volts and polarity as shown, should be presented at the output. The ON + OFF period should be approximately 100 + 100 mSec. If this output is correct check the second output winding. Check that the ON time decreases as the control input is reduced to -4V. Check that the ON time increases as the control input is increased to -9V.
4. If no pulses are present at the output, set the control input to -6.5V and monitor the signal at T3 collector with the oscilloscope. This should be a square wave of period approximately 100 + 100 mSec switching between 0V and -9V. If this square wave is present check operation of T4 and the output blocking oscillator. If the square wave is not present at T3 collector check operation of T1, T2, T3. The d.c. voltage table will assist on locating the fault.

D.C. VOLTAGE TABLE.

Typical d.c. voltages for the transistors are given in the table. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

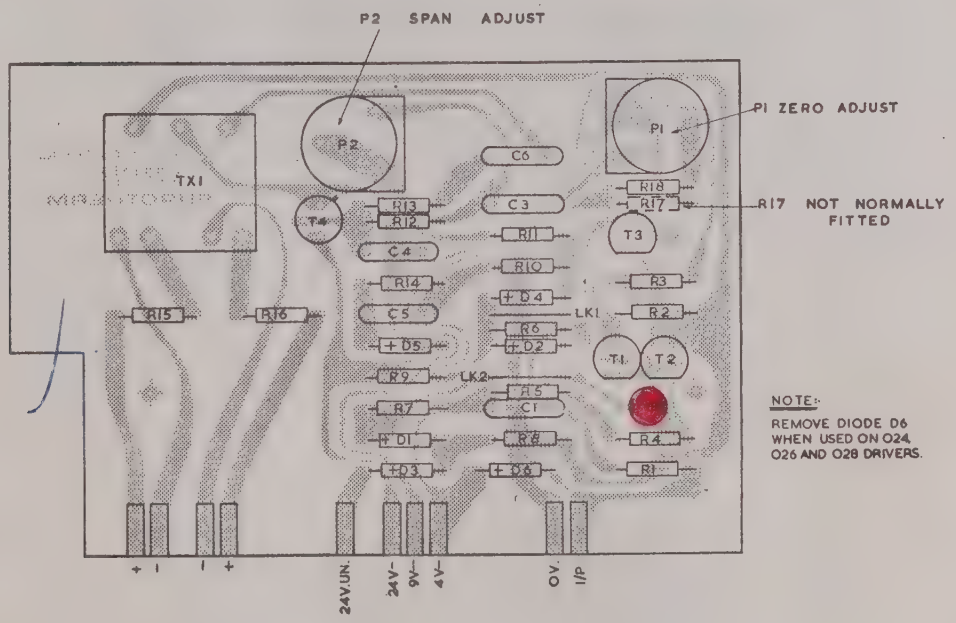
	CONTROL INPUT	T1	T2	T3	T4
EMITTER	-4V -9V	-4.5V -9V	-4.5V -9V	0V 0V	0V 0V
BASE	-4V -9V	-4V* -9V*	-4V* -9V*	-.7V 0V	0V +.5V
COLLECTOR	-4V -9V	-7V 0V	0V 0V	0V -9V	-28V -28V

* Must be measured with an oscilloscope or an electronic voltmeter due to the high circuit resistance.
All other measurements may be taken with a d.c. voltmeter having a resistance of 20KΩ/Volt.
All voltages measured with reference to 0V.



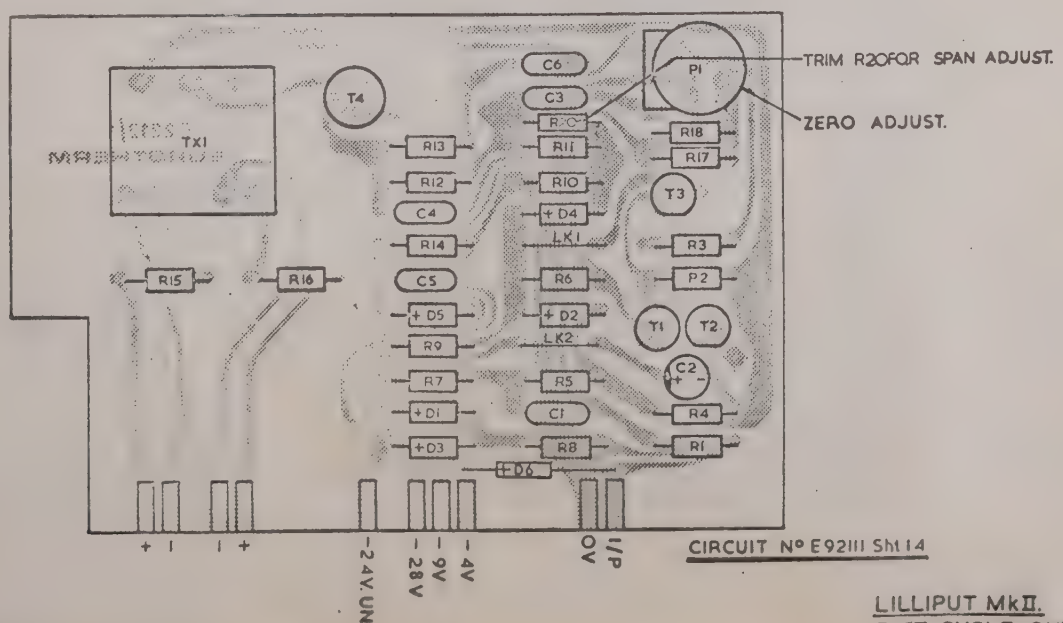
LILLIPUT MkII.
FAST CYCLE OUTPUT.

Drg NºE92111 Sht14



LILLIPUT MK2
FAST CYCLE OUTPUT
CIRCUIT No E92111sht14

Drg No D93240 Issue 2



CIRCUIT Nº E92111 Sht14

Drg Nº D93240R

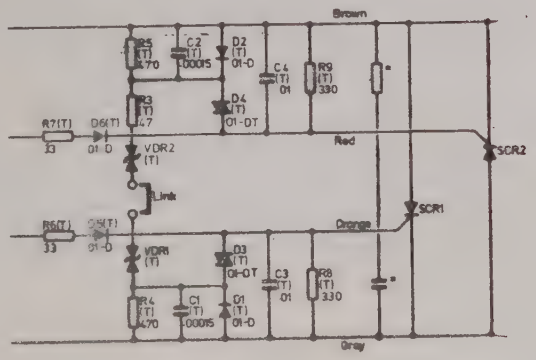
LILLIPUT MkII.
FAST CYCLE OUTPUT.

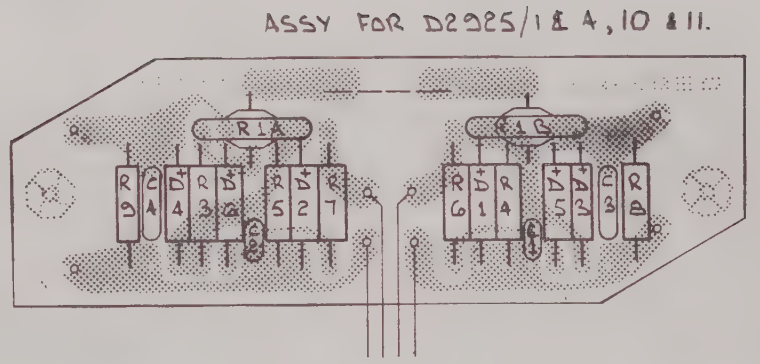
SCR PROTECTION CIRCUIT

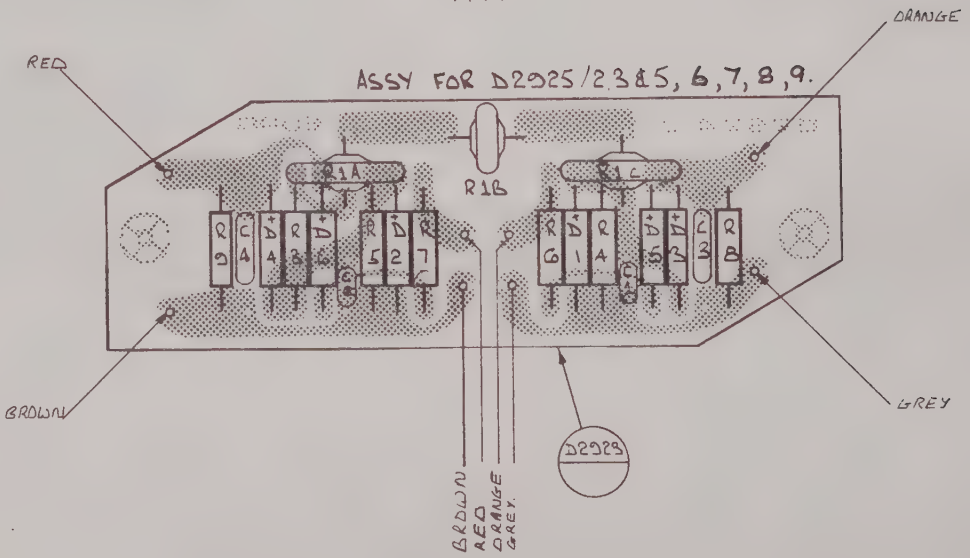
Function. SCR's are connected in inverse parallel pairs. A protection circuit is provided to prevent damage to the SCR's by supply transients. The p.c.b. is mounted on the SCR stack.

Circuit description. A supply voltage surge will trigger the forward biased SCR into conduction, thus preventing a high reverse voltage being applied to the other SCR. The normal trigger pulses are fed to the SCR gates via R6, D5 and R7, D6. Non linear resistors VDR1 and VDR2 reduce in value at high voltages allowing current to flow in R4 or R5. Thus capacitor C1 or C2 charges to a voltage defined by the potential across either R4 or R5 depending on the sense of the transient. Whilst one capacitor is being charged the other is clamped to 0.6V by diode D1 or D2 in parallel with the capacitor. As C1 or C2 charges an increasing voltage is applied to the associated diac which has a very high forward resistance until the break-over voltage of the device is reached (about 35V). At this point the diac will display negative resistance and will conduct heavily causing SCR gate current to flow. The diac thus ensures that the protection gating signals are of sufficient amplitude to cause the SCR to conduct. Diodes D5 and D6 prevent protection gating current flowing through R6 and R7.

Filters formed by C3, R8 and C4, R9 prevent spurious triggering of the SCR by noise voltages. A fast acting series fuse protects the SCR from current overload.

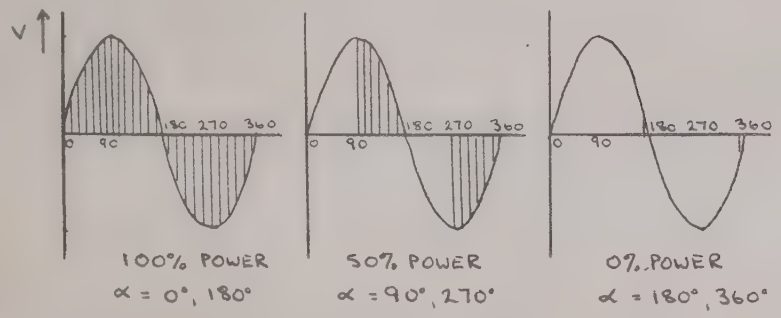






Phase Angle Output Board (002)

Phase angle control is the process of rapid ON-OFF switching that connects an A.C. supply to a load for a controlled fraction of each cycle. The phase angle, α, at which the S.C.R.'s are triggered into conduction is 0° (fully advanced) for maximum power and 180° (fully retarded) for minimum power.



Function

The phase angle output board accepts an input control signal operating between -4V for zero power and -8.2V for maximum power. The output is two sets of trigger pulses suitable for firing an inverse parallel pair of S.C.R.'s in the phase angle mode. Soft start circuitry prevents large inrush currents into the load by slowly advancing the phase angle from fully retarded. In addition, there is a current limit option that allows maximum load current to be set between 25% and maximum rated current by an external 47K variable resistor. Included as standard, power feedback immediately compensates for supply voltage fluctuations, eliminating the need for a change in load temperature to produce a correcting error signal.

Circuit Description

The circuit consists of a pulse width modulator TR1-TR4 and associated components feeding a blocking oscillator, TR5 and associated components.

Pulse Width Modulator

The mark to space ratio of the rectangular output waveform at TR4 collector increases from zero for a control signal input of -4V to infinity for a control signal of -9V.

The control signal is fed via R3 to the input at TR1 base of the integrator formed by TR1 and C2. The output at TR1 collector forms a pedestal that ramp generating capacitor C3 charges from. The base of supply voltage synchronising switch TR2 is fed from a potential divider between the +28V smoothed rail and the -24V unsmoothed rail. During the zero voltage crossover point of the mains supply cycle, TR2 turns on discharging C3 to the 0V rail. When TR2 turns off, both plates of C3 move positively, due to the presence of R13, until D4 becomes forward biased clamping the negative plate of C3 to the pedestal integrator output. In this condition, D5 is reverse biased and the positive plate of C3 ramps positively as C3 charges via R13. When C3 charges to 9V the comparator TR3, TR4, D7 changes state, turning on the blocking oscillator. The mark to space ratio of the rectangular waveform at TR4 collector stabilises when the average negative feedback current through P2 and R9 is equal to the current through R3.

When the control signal is -4V, corresponding to a power demand of zero, the pedestal integrator output is +4V. The time constant of the R13, C3 combination is such that the voltage on C3 just fails to reach the +9V, necessary to switch the comparator during the 10m secs of the mains half cycle. However, with a control signal of -9V, the pedestal integrator output is +8V and the comparator switches as soon as TR2 turns off at the beginning of the half cycle.

D3 clamps the output of the pedestal integrator to about 9V enabling the soft start circuit to be fully effective for all conduction angles. D4 and D5 isolate the output of the integrator when TR2 discharges C3. D6 prevents excessive reverse bias being applied to TR2 base. D7 prevents the flow of reverse base - emitter current when TR4 is off. D8 clamps the negative output excursion of the pulse width modulator to -0.6V.

C8 (0), shown in the power supply section of the overall circuit diagram, generates a +28V smoothed rail from the normal +24V unsmoothed rail. R16 (0) and Z1 (0) provide a +8.2V reference for the pulse width modulator and current limit circuits.

Blocking Oscillator

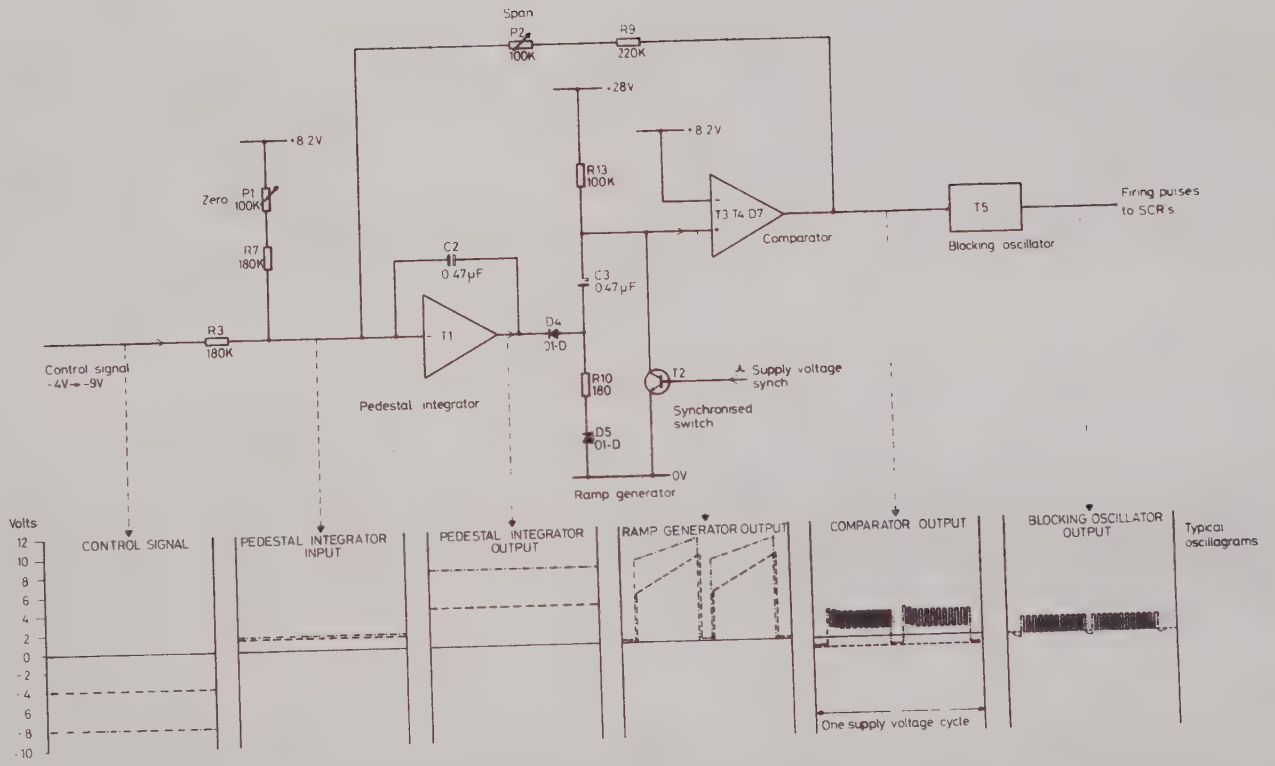
The blocking oscillator formed by TR5, the pulse transformer and associated components produces SCR firing pulses at the output windings of amplitude 10V, duration 12μ secs and repetition rate 4 pulses per m sec.

TR5 conducts when the output from the pulse width modulator is high. Current flows through the lower half of the primary winding inducing a current in the upper bias winding, which is transmitted as a positive feedback signal through C7 and R18 to the base of TR5, driving TR5 into saturation. After 12μ secs, C7 is fully charged via R18 and TR5 base - emitter junction. TR5 stops conducting whereupon the transformer core flux collapses and the reverse current flow in the transformer primary windings drives TR5 into cut-off.

TR5 conducts again after approximately 250u secs when C7 has discharged through R18, R17 and R22. The trigger pulses cease at the end of the mains half cycle when TR4 turns off. D9 and R19 clip the negative pulse caused by inductive reversal of the primary current, thereby protecting TR5 from excessive reverse base-emitter voltage. R17 and C4 form a low pass filter that partially smoothes the pulses fed back from the blocking oscillator to the pulse width modulator. C5 prevents spurious triggering of the oscillator by noise.

Soft Start

Network R5, R6, C1, D1 and D2 ensures that after an interruption of supply voltage the phase angle is slowly advanced from 180°. This eliminates current surges, particularly troublesome with inductive loads.


Span
P2
100K
R9
220K
+28V
+8.2V
+8.2V
R13
100K
Zero
P1
100K
R7
180K
C2
0.47μF
C3
0.47μF
T3 T4 D7
Comparator
T5
Blocking oscillator
Firing pulses
to SCR's
R3
180K
D4
01-D
T1
Control signal
-4V→-9V
Pedestal integrator
R10
180
T2
Supply voltage
synch
Synchronised
switch
D5
01-D
0V
Ramp generator
Volts
12
10
8
6
4
2
0
-2
-4
6
-8
-10
CONTROL SIGNAL
PEDESTAL INTEGRATOR
INPUT
PEDESTAL INTEGRATOR
OUTPUT
RAMP GENERATOR OUTPUT
COMPARATOR OUTPUT
BLOCKING OSCILLATOR
OUTPUT
Typical
oscillagrams
One supply voltage cycle

Diode D1 is normally forward biased causing D2 to remain reverse biased. The small charge on C1 prevents D2 from conducting when the unsmoothed -24V rail falls to zero during the zero voltage crossover point of the supply cycle. If the instrument supply is interrupted the -24V rail ceases immediately but the +28V rail remains due to the charge on C8. Diode D2 rapidly discharges C2, fully retarding the conduction angle.

Current Limit

The input of the pedestal integrator is held at +0.6V by the base-emitter voltage drop of TR1. Potential divider R1, R2 provides a +0.6V reference so that a current limit input signal of only 100mV is sufficient to turn off the output pulses even with a maximum power demand.

Power Feedback

Load power is directly proportional to the square of the supply voltage. The voltage across C8 will increase by 10% for a 10% increase in supply voltage. The consequent change in current through R14 causes the collector voltage of TR4 to rise by approximately 20%. The resulting increase in feedback current decreases the mark-to-space ratio of the rectangular output waveform, thereby compensating for the change in supply voltage.

Calibration and Checking

Calibration

1. Remove link d1 - d2 and make link I1 - I2 on the amplifier board. Connect a multimeter set to the 10V range between the I1 - I2 link and the -4V rail to monitor the control signal. Set the power pot, P4 (A) fully clockwise to maximum.

2. Connect an oscilloscope to one of the pulse transformer output windings. Connect a mV source and mains leads to the appropriate terminals. Switch on the instrument and allow it to warm up for 20 minutes.

3. Adjust the set point and/or mV source so that the control signal is zero. With the normal supply voltage adjust P1 (O) so that output pulses are produced and then turn the pot clockwise so that the pulses just cease.

4. Adjust the set point and/or mV source so that full power is demanded. Increase the supply voltage by 10% and adjust P2 (O) to give maximum pulse output.

5. Repeat 3 and 4 until a consistent result is obtained.

6. Check the polarity of both sets of output pulses. The amplitude in the unloaded state will be about 10V.

7. Remove the I1 - I2 link and replace the d1 - d2 link.

Fault Location

If a fault is suspected :

1. Check the power supply rails + 28V smoothed, +8.2V, OV, -4V, -9V, -24V unsmoothed and -28V smoothed.

2. Check that the control signal varies between -4V and -9V. If the control signal range is incorrect remove the output board and re-check. If the control signal is now normal then the output board must be loading it. If however the control signal is still incorrect then the fault does not lie on the output board and must be traced back through the circuit.

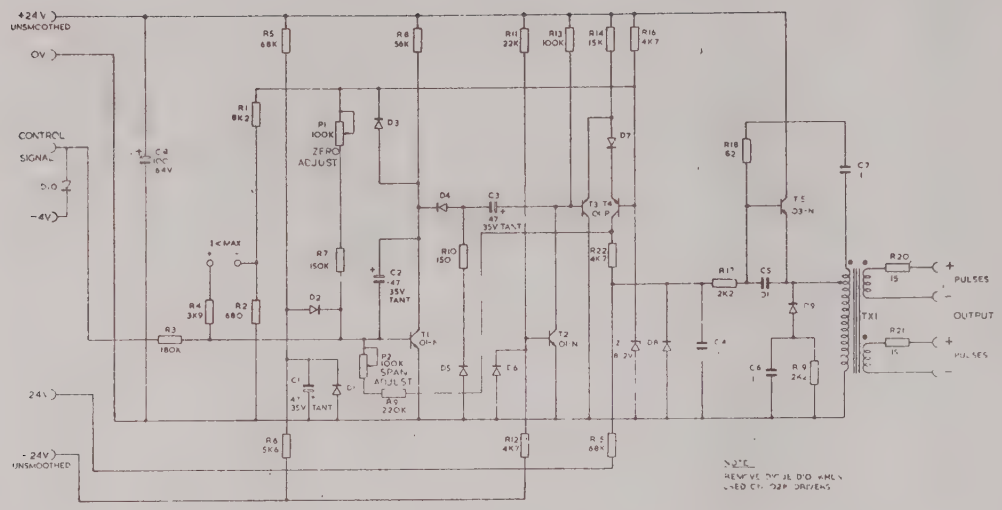
3. Connect the oscilloscope between OV and TR1 collector. The collector potential should increase from between +3V and +4V with a -4V control input to +8V with a -9V control input. If this is correct, connect the oscilloscope between OV and the base of TR2. A positive pulse of amplitude 1.5V and duration 1 mSec should occur once every 10 mSec if the mains supply is 50 Hz. If this is correct, connect the oscilloscope between OV and the collector of TR2. The waveform should be a positive ramp which returns to OV at every crossover point in the mains cycle (every 10 mSec for a 50 Hz. supply). The d.c. level at which the ramp commences should increase as the input control signal is increased from -4V to -9V. If this is correct, connect the oscilloscope between OV and the junction of R22 and R15. The waveform should be a square wave of amplitude 3 volts, the positive period increasing from zero to approximately 90% as the input control signal is increased from -4V to -9V. Some 2 volts of high frequency oscillation will be superimposed on the positive part of the waveform due to the action of the blocking oscillator. If the waveform is normal and the pulse output is not, check operation of TR5 and the output blocking oscillator. The d.c. voltage table will assist in locating faults, particularly if an oscilloscope is not available.

D. C. Voltage Table

Typical d.c. test voltages for the transistors are given in the table. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

	CONTROL INPUT	TR1	TR2	TR3	TR4	TR5
EMITTER	-4V	OV	OV	+6V*	+5.5V*	OV
	-9V	OV	OV	+8V	+7.5V	OV
BASE	-4V	+.6V	-.5V	+5V*	+8V	-.5V
	-9V	+.6V	-.5V	+10V*	+8V	-.7V
COLLECTOR	-4V	+2V*	+2V*	OV	-.5V*	+30V
	-9V	+8V*	+8V*	OV	+4V	+30V

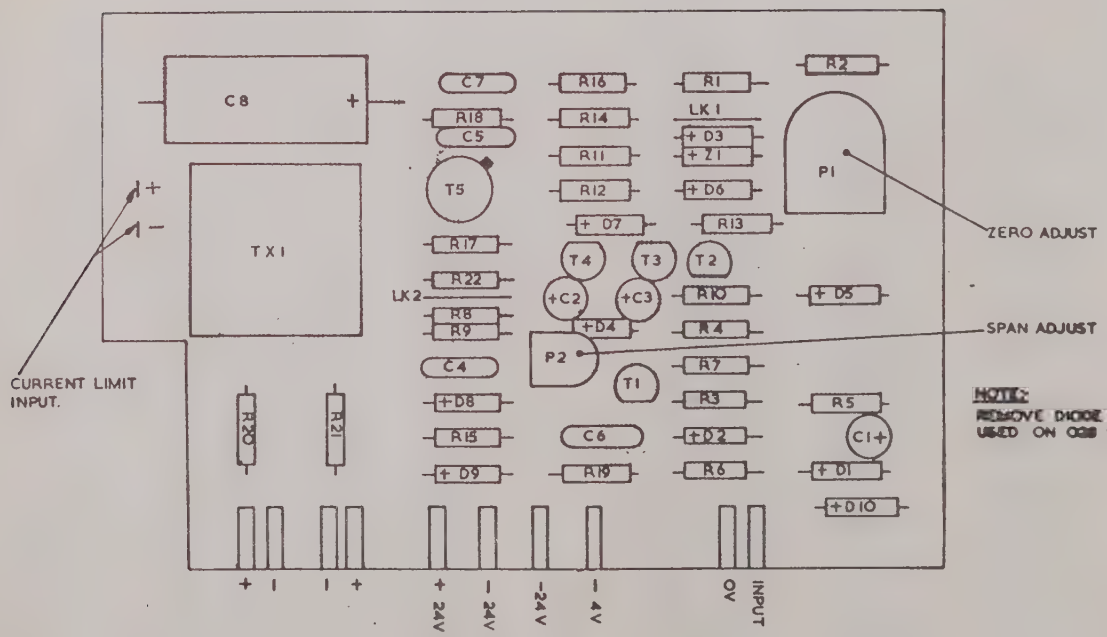
* These voltages are dependent on setting of P1
All voltages measured with reference to OV using a d.c. voltmeter having a resistance of 20KΩ/volt.



LAYOUT Nº D93253

LILLIPUT MkII
PHASE ANGLE OUTPUT

Drg Nº E92111 Sht 15



LILLIPUT MkII
PHASE ANGLE OUTPUT
CIRCUIT No E92111 Sheet 15

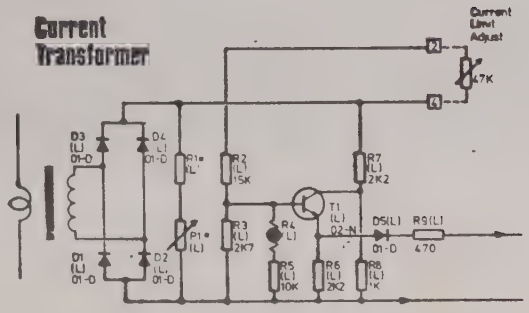
Drg No D93253

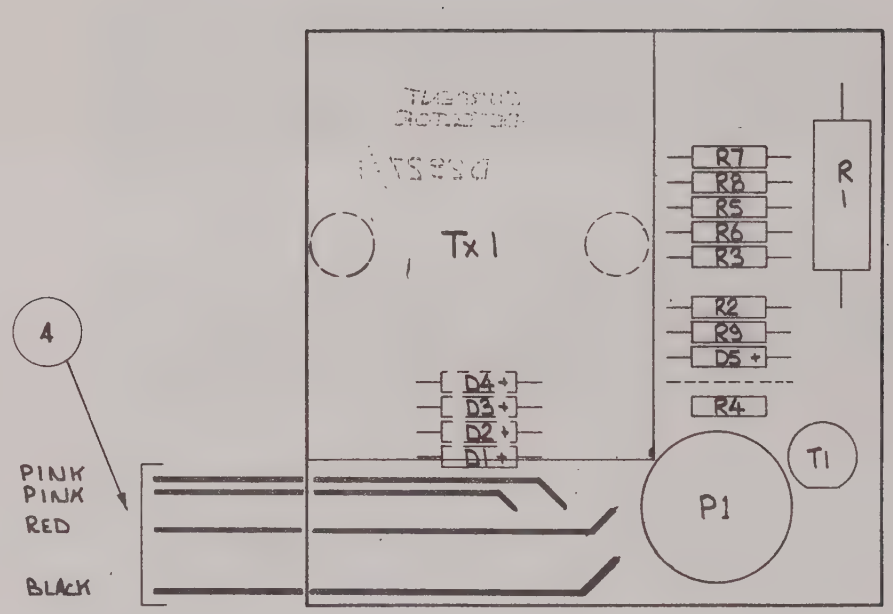
CURRENT LIMIT BOARD (OPTION 42)

Function. The current limit circuit samples the load current and at a predetermined level converts the resulting d.c. voltage to a feedback current. Provision for fixed or variable limit control is made by connection to the rear terminals of a fixed or variable resistance.

Circuit description. The primary winding of transformer TX1 is connected in series with the load. The secondary output is full wave rectified by D1 to D4 and is applied across R1 and P1 to provide collector potential to transistor T1. The collector potential is taken from the junction of R7 and R8 and emitter current is supplied through R6. Base bias is taken from the junction of R2 and R3 both of which are connected in series with an external 47K resistor. The bias chain is connected across the rectified transformer output. Base potential is thermally stabilized by thermistor R4 and resistor R5.

A rise in load current is detected and by emitter follower action is transferred as a corresponding rise in potential at T1 emitter. When the potential at T1 base reaches the conduction threshold diode D5 conducts allowing current to flow through R4 on the output board. This current bleed will limit the drive to the output board which will in turn limit the load current. The value of load current for which D5 will conduct is determined by the value of the base bias resistance chain. The 47K resistor, which is connected across rear terminals 2 and 4, gives fixed current limiting at the maximum rated current. This resistor may be replaced by a 47K potentiometer which will allow control of the current limit level.





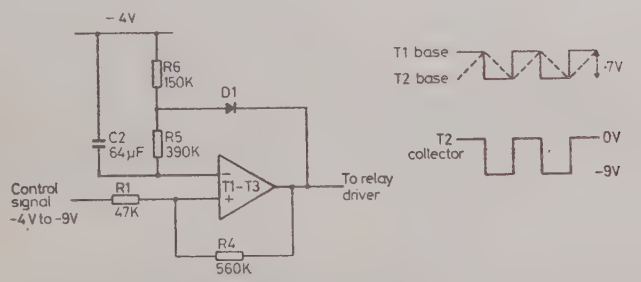
RELAY OUTPUT BOARD. (003, 026 and 028)

Function

The relay output board converts a 0 to 5V d.c. input signal into a time proportioning relay output.

Circuit Description

The input control signal operates between the levels -4V and -8.2V corresponding respectively to minimum and maximum relay ON time. Provision is made for reversing this action for cooling applications, the -4V and -8.2V input levels then corresponding respectively to maximum and minimum relay on time. The output relay is energised on a time proportioning basis with an ON + OFF period of approximately 10 + 10 seconds at 50% output. For electrical heating applications power feedback is normally included so that the load power remains constant if the mains voltage varies. For cooling applications the power feedback feature is normally omitted. A spark suppression network R15, C3 is provided across the normally-open output contact.



Transistors T1 to T3 and associated components form a high-gain d.c. amplifier with overall positive gain from T1 base to T3 collector and positive feedback via R4. With an input control signal of -7V to R1, transistors T1 and T3 switch off and the collector of T3 falls to a potential of approximately -9V as defined by the current through T5 R11 D3, R17 when the board is operating in the normal mode. Positive feedback via R4 causes the potential at T1 base to fall to -7.2V. Diode D1 conducts, causing capacitor C2 to charge negatively towards -9V (T3 collector potential) via R5. When C2 has charged to -7.2V, transistors T1 and T3 conduct and T3 collector potential rises to 0V. Positive feedback via R4 causes T1 base potential to rise to -6.5V ensuring that T1 and T3 remain hard on. Diode D1 is reverse biased and C2 commences to discharge towards -4V via R5, R6. Capacitor C2 discharges to -6.5V after approximately 10 seconds, at which point transistors T1 and T3 switch off. The positive feedback via R4 causes T1 base potential to fall again to -7.2V and capacitor C2 charges negatively from -6.5V towards -9V (T3 collector potential) via R5, D1. Capacitor C2 charges to -7.2V after approximately 10 seconds, at which point T1 and T3 conduct and the cycle is repeated. With an input control signal of -7V capacitor C2 thus charges and discharges continually between the levels of -6.5V and -7.2V producing a square wave of period approximately 10+10 seconds and magnitude approximately 9 volts at T3 collector. In the normal mode, with T4 R8, R9, D2 omitted and Lk1 made, transistor T5 and the output relay switch on whenever T3 collector is negative.
The ON-OFF switching differential of .7V at T1 base remains approximately constant as the input control signal varies, but the switching level follows the control signal. As the input control signal becomes more negative the average level of charge on C2 becomes more negative, causing the charging current via D1 to decrease and the discharge current to increase. This gives an increasing relay ON time and a decreasing relay OFF time until the output relay stays permanently ON when the control signal becomes more negative than T3 collector potential (approximately -9V). As the input control signal becomes less negative the output ON time decreases and the OFF time increases until the relay stays permanently OFF with an input control signal of less than -4V.

Power Feedback

Due to the square law relationship between voltage and power, a 10% rise in mains voltage will produce a 20% rise in load power with electrical resistance heating unless the output ON time reduces by 20% to compensate for the change. A 10% rise in mains voltage causes a 10% rise in smooth, but unstabilised, -28V supply. This produces a 10% change in T3 collector voltage from -9V -9.9V during the period when the output relay is ON. The increased charging current through R5, D2 reduces the output ON time by approximately 20% and thus compensates for the change in supply voltage. For correct mains voltage compensation in the normal mode, with T4, R8, R9, omitted and LK1 made, diode D2 must also be omitted. Inclusion of D2 in this mode will not remove power feedback but merely reduce it to an incorrect level.

Inverted Relay Mode

For cooling applications the mode of operation of the output relay can be inverted by including components T4, R8, R9, D2 and omitting LK3. When T3 collector falls to -9V transistor T4 is switched on and the relay is de-energised The relay energises when T3 collector rises to 0V and T4 becomes non-conducting Inclusion of diode D2 clamps the junction R7, R18 at -9.5V and the correct feedback level of -8.5V at T3 collector is established by the potential divider R9, R18. Inclusion of Diode D2 stabilises T3 collector potential against mains variations of the -28V supply and thus eliminates power feedback, this being an undesirable feature for cooling applications.

Relay Output Stage.

Diode D4 provides a path for the inductive current of the relay coil when the relay is de-energised to protect T5 from excessive voltage. The spark suppresion network consisting of filter C3, R15 can be connected across the normally open relay contact to absorb the inductive current of an external contactor coil. The second relay contact is used to operate the facia mounted neons. In the normal mode the red neon illuminates when the relay is energised and the green neon illuminates when the relay is de-energised.

Calibration Procedure.

1. Demand maximum output from the 3 term amplifier with link I1, I2 made and d1, d2 open circuit. Attach a voltmeter between link I1, I2 and -4V and adjust the power pot P4 on the amplifier board to give a zero reading on the meter. Replace link 2 on the o/p board with a 0.22uf capacitor to speed up relay cycle time, and adjust P1 on the o/p board to just give zero power output green neon alight on facia.
2. Demand maximum power from 3 term amplifier with P4 increase mains voltage by 10% and adjust P2 to give maximum output,red neon alight on facia.

Checking

1. With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -4V, -9V, -24V and -28V supplies with a d.c. voltmeter. Failure of any of the power supplies could be due to a mother board or amplifier board fault. Plug in calibration board and connect an input to the controller.
2. Connect a 10V d.c. voltmeter between the control input and OV terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.
3. Set the input control signal to -6.5V and observe the operation of the output relay. The relay should cycle with an ON + OFF period of approximately 10 + 10 seconds and the red and green facia-mounted neons should light when the relay is energised and de-energised respectively. If the board is connected in the normal mode check that the relay ON time increases to maximum as the control input increases to -9V and that the relay ON time decreases to minimum as the control input is reduced to -4V. If the board is connected in the inverted mode check that the relay ON time decreases to minimum as the control input is increased to -9V and that the relay ON time increases to maximum as the control input is reduced to -4V.
4. If the relay fails to cycle, set the control input to -6.5V and monitor the signal at T3 collector with the voltmeter. This signal should switch between OV and -9V approximately once every 10 seconds. If this signal switches normally, check operation of T5, RL1 or T4, T5, RL1 depending on the mode of operation. If the signal at T3 collector is not correct check operation of T1, T2, T3. The d.c. voltage table will assist in locating the fault.

D. C. Voltage Table

Typical d.c. test voltage for the two operating modes are shown in the table. With the output board, calibration board and the main amplifier board inserted in the mother board, demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

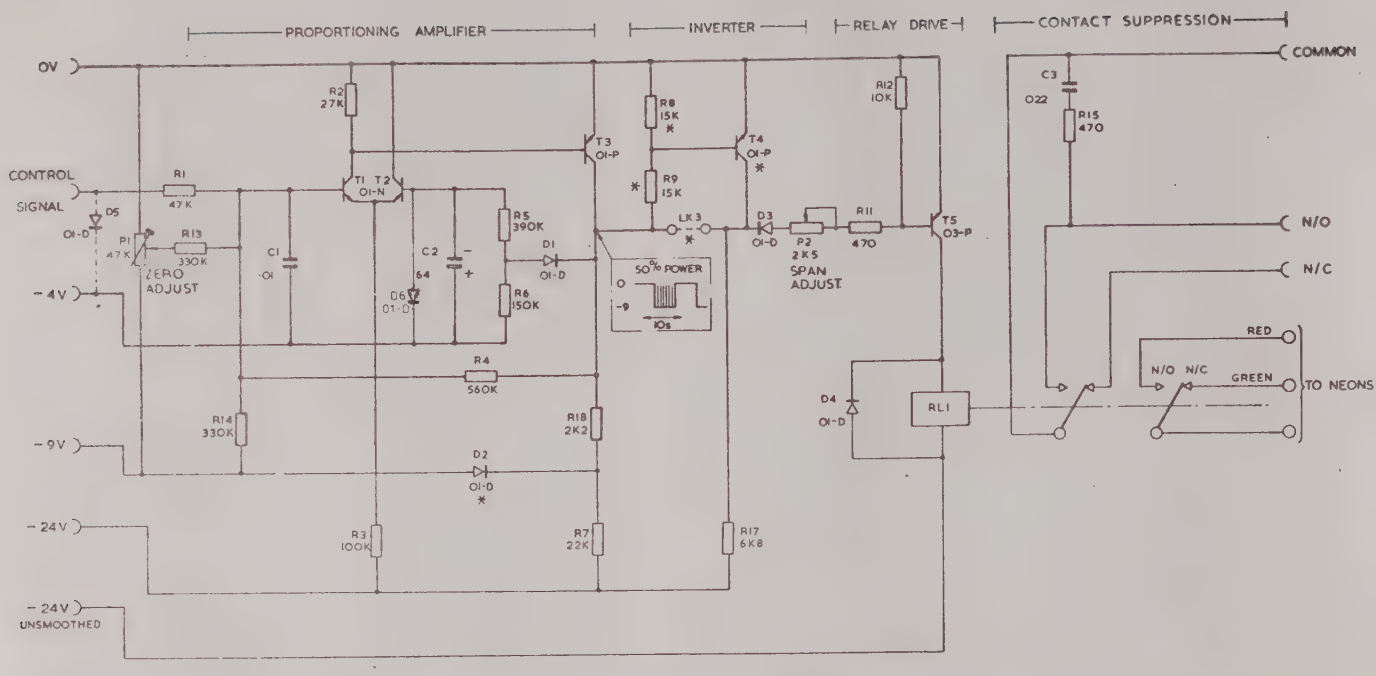
Normal

	CONTROL INPUT	T1	T2	T3	T5
EMITTER	-4V -9V	-4.5V -9V	-4.5V -9V	OV OV	OV OV
BASE	-4V -9V	-4V* -9V*	-4V* -9V*	-.7V OV	OV -.7V
COLLECTOR	-4V -9V	-.7V OV	OV OV	OV -9V	-28V OV

Inverted

T4	T5
OV	OV
OV	OV
OV	-.7V
-.7V	OV
-9V	OV
OV	-28V

* Must be measured with an oscilloscope or an electronic voltmeter due to high circuit resistance.
All other measurements may be taken with a d.c. voltmeter having a resistance of 20KΩ/Volt.
All voltages measured with reference to OV.

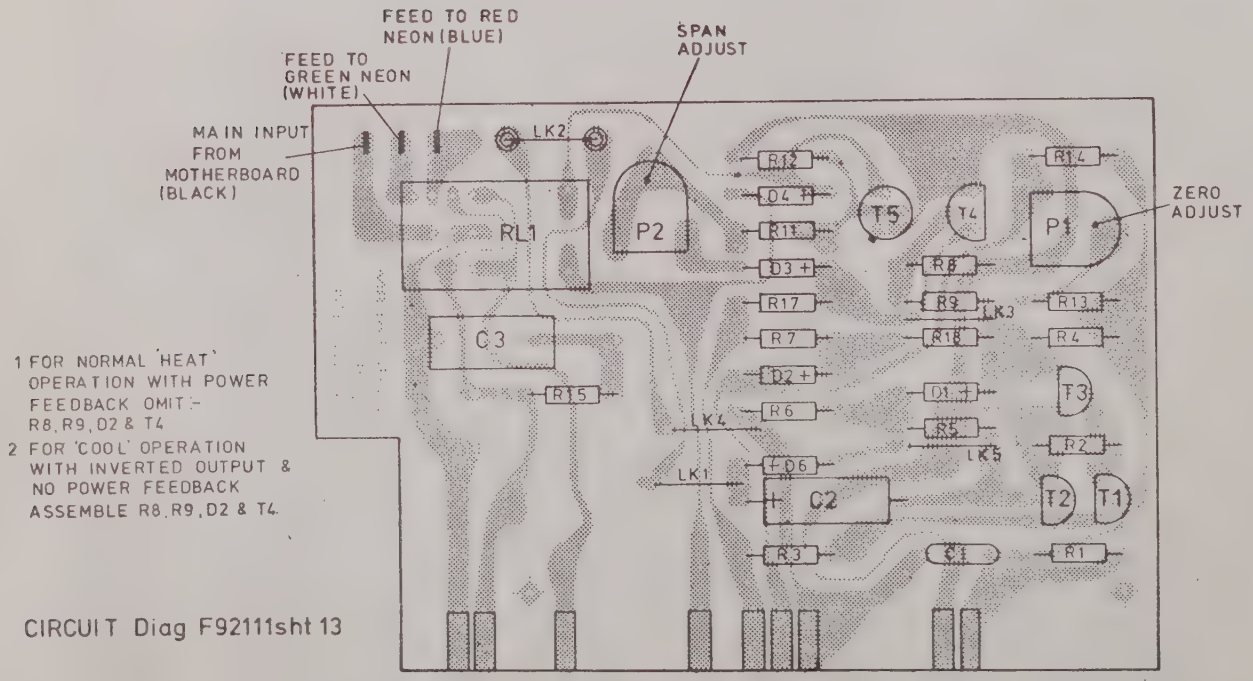


COMPONENTS MARKED THUS * VARY WITH MODE OF OPERATION
FOR NORMAL OUTPUT, ASSEMBLE LK 3 & NOT R8, R9, T4.
FOR INVERTED OUTPUT, ASSEMBLE R8, R9, T4 & NOT LK. 3
FOR POWER FEEDBACK OPERATION DO NOT ASSEMBLE D2

LAYOUT Nº D93164

LILLIPUT Mk II.
RELAY OUTPUT.

Drg Nº E92111 Sht 13



1 FOR NORMAL 'HEAT' OPERATION WITH POWER FEEDBACK OMIT :- R8, R9, D2 & T4
2 FOR 'COOL' OPERATION WITH INVERTED OUTPUT & NO POWER FEEDBACK ASSEMBLE R8, R9, D2 & T4.

CIRCUIT Diag F92111sht 13

LILLIPUT MK II
RELAY OUTPUT.

Drg No D93164

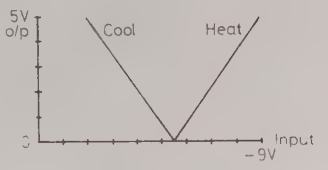
DUAL 5 VOLT OUTPUT BOARD. (007)

Function

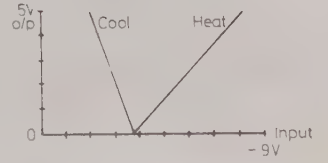
The dual 5 volt output board converts a -2 to -8.5 volt d.c. input into two electrically isolated 0 to 5 volt d.c. outputs with a current rating of .25mA. The board has a special input-output characteristic intended for heat-cool applications.
The input control signal operates between the levels -2V and 8.5V. An input of -2V corresponds to maximum 5 volt cool output and zero heat output. An input of -8.5V corresponds to zero cool output and maximum 5 volt heat output. The input-output characteristic is such that the cooling output falls gradually to zero as the input signal becomes more negative and the heat output then increases gradually from zero. The changeover from cooling to heating can be made to occur anywhere within the input signal range -4V to -7V by adjusting the rear-access 'relative-bandwidth' control P1. The heat and cool outputs can be made to overlap by up to 5% at the changeover point by adjusting the rear access -'overlap' or 'crossover' control P4.

Relative bandwidth

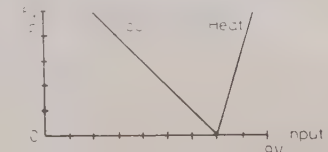
The setting of the proportional band potentiometer P1 on the main amplifier board defines the amplifier input change, expressed as a percentage of span. required to give an amplifier output change from -4V to-8.7V, these two levels corresponding to zero and maximum output respectively for the majority of output boards. Since the dual 5 volt board requires a control signal from -2V to -8.5V to give an output change from maximum cooling to maximum heating, the total bandwidth between the maximum cooling and maximum heating points is 1.4Xp where Xp is the amplifier bandwidth setting.
For satisfactory heat-cool operation the heat channel gain expressed in watts per degree change, should match the cool channel gain. The relative bandwidth control enables the heat channel gain to be increased as the cool cool channel gain is decreased, and vica-versa. This enables the heat and cool channels to be matched provided the external parameters of the separate channels do not differ by a factor or more than10:1.
With the relative bandwidth control P1 set midway the heat and cool channel bandwidths are equal at approximately .7Xp and crossover occurs at an input of approximately -5.5V.



With the relative bandwidth control P1 set fully anticlockwise the heat channel bandwidth is approximately three times wider than the cool channel band - width and crossover occurs at an input of approximately -4V.

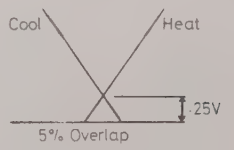


With the relative bandwidth control P1 set fully clockwise the cool channel band-width is approximately three times wider than the heat channel bandwidth and crossover occurs at an input of approximately -7V.

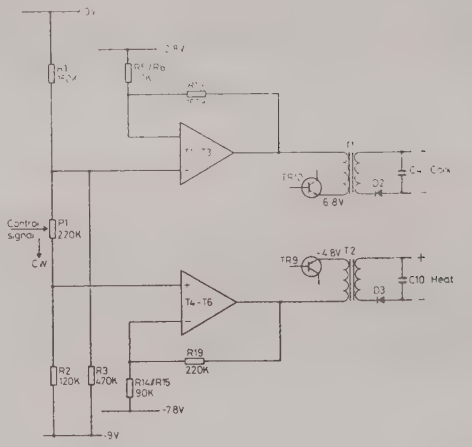


Overlap

Some overlap of the heat and cool channels is provided so that the effect of any external driver imperfection or channel gain mismatch can be minimised in the crossover region. With the overlap or crossover control P4 set fully anticlockwise there is no overlap and the heat output increases from zero as soon as the cool output falls to zero. With the overlap control set fully clockwise there is 5% of overlap of heat and cool channels, an output of .25 volts being present on both channels at the crossover point.



Circuit Description



The cool oscillator consisting of T7, TX1 and associated components derives its negative supply from emitter follower T10 and its positive supply from the cool amplifier consisting of T1 to T3 and associated components. The heat oscillator consisting of T8, TX2 and associated components derives its positive supply from emitter follower T9 and its negative supply from the heat amplifier consisting of T4 to T6 and associated components. The oscillators have equal primary and secondary turns and the output voltage is thus equal to the oscillator supply voltage minus the .5V diode drop. With zero overlap the emitter potentials of T10 and T9 are held respectively at -6.8V and -4.8V.

The cool amplifier has a positive gain of 3.2 from T1 base to T3 collector as defined by the values of R5, R6, R10. A reference potential of -2.8V is provided at T2 base by potential divider R5, R6. A potential of -2.1V at T1 base corresponds to a cool amplifier output of -0.6V a cool oscillator supply of 6.2 volts and a cool output of 5.7 volts. With maximum output loading of .25mA the cool output decreases to 5 volts due to regulation. A potential of -3.8V at T1 base corresponds to a cool amplifier output of -6.3V, a cool oscillator supply of .5 volt and a cool output of zero. With maximum load the cool output thus decreases from 5 volts to zero as the potential at T1 base falls from -2.1V to -3.8V.
The heat amplifier has a positive gain of 3.5 from T4 base to T6 collector as defined by R14, R15, R19. A reference potential of -7.8V is provided at T5 base potential divider R14, R15. A potential of -7V at T4 base corresponds to a heat amplifier output of -5.3V, a heat oscillator supply of .5 volt and a heat output of zero. A potential of -8.5V at T4 base corresponds to a

heat amplifier output of -10.3V, a heat oscillator supply of 5.5 volts and a heat output of 5 volts. The heat output thus increases from zero to 5 volts as the potential of T4 base falls from -7V to -8.5V.
The input network consisting of P1, R1, R2, R3 holds the bases of T1 and T4 at -3.8V and -7V respectively in the absence of an input signal i.e. with the input open circuit. The heat and cool channels are therefore, both biased to a point where they are just giving zero output. When a control signal is applied to the wiper of P1, a positive shift in the base potentials of T1 and T4 causes the cool output to increase and the heat output to remain zero and a negative shift in the base potentials of T1 and T4 causes the heat output to increase and the cool output to remain at zero. The influence of the control signal on the bases of T1 and T4 is dependent on the setting of P1 due to the potential divider action of P1 with R1 and R2. The relative gains of the heat and cool channels are thus dependent on the setting of P1. When the resistance of the overlap control P4 is set to maximum the emitter potential of T9 is shifted positively by 0.25 volts and the emitter potential of T10 is shifted negatively by 0.25 volt. With no input signal applied the output on both heat and cool channels is thus 0.25 volt, giving 5% overlap of heat and cool outputs.
The cool oscillator consisting of T7, TX1 and associated components is biased into conduction by current through R26, giving base drive to T7 which is proportional to the oscillator supply voltage across C3, provided the voltage across C3 is of the correct polarity. Positive feedback to T7 base via C7, R27 and the bias winding of TX1 causes the circuit to oscillate at a frequency of 30KHz defined by the parallel tuned circuit consisting of C5 and the primary inductance of TX1. Resistor R30 provides base drive to T7 when the voltage across C3 is small ensuring that oscillation commences at very low applied voltages. Resistor R24 limits T7 peak collector current and ensures sinusoidal oscillation. The peak value of oscillation on the primary of TX1 is only slightly less than the oscillator supply voltage across C3 (the peak to peak voltage is twice this value). The secondary winding has a few more turns than the primary to allow for the forward voltage drop across diode D2. The peak rectifying and smoothing network D2, C9 thus gives a d.c. cool output voltage which is nearly equal to the d.c. voltage across C3. The heat oscillator operates in a similar manner.

Adjustment

The adjustment potentiometers P2 and P3 are factory set and should not be disturbed unnecessarily. If adjustment is necessary the following procedure must be adopted.

1. Open circuit the control signal input by opening the link on the output board. Insert the output board into the mother board and ensure that the main amplifier board is also present.
2. Place a d.c. voltmeter across each of the 5 volt outputs and apply the normal load to each output. Set the'crossover' or 'overlap' control P4 fully clockwise.
3. Connect the supply and adjust P2 until equal readings are obtained on both outputs. Adjust P3 until the sum of the output readings is equal to .5 volt. Re-adjust P2 and P3 until an output of .25 volt is obtained simutaneously on each channel.
4. Remake the control signal link and set P4 fully anticlockwise.

Checking

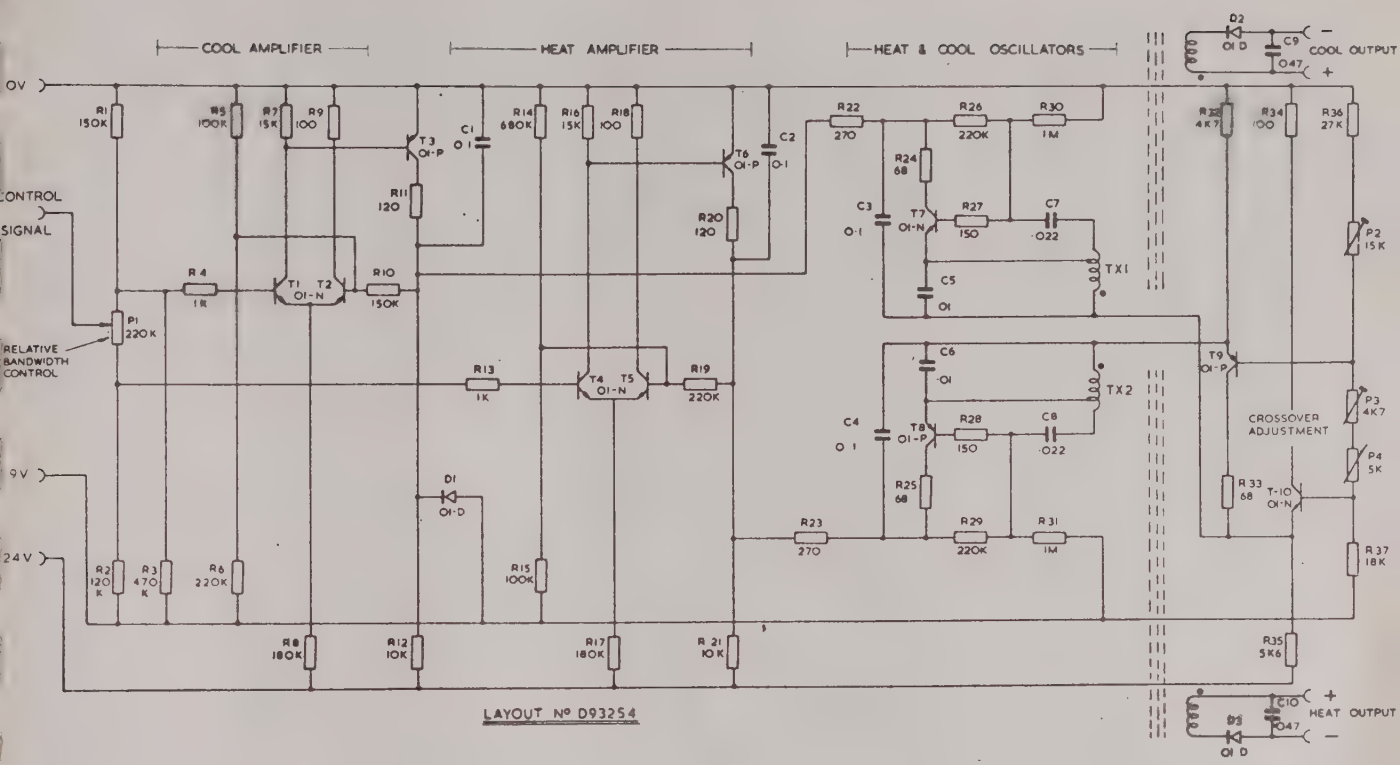
1. With the output board and the main amplifier board inserted in the mother board, connect the mains and check the -9V and -28V supplies. Failure of a power supply could be due to a fault on the mother board or the amplifier board.
2. Connect a d.c. voltmeter between the control input and OV terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.
3. Place a 10V d.c. voltmeter across each of the 5 volt outputs and supply the normal load to each output. Set the relative 'bandwidth' control P1 to its mid position. Set the 'overlap' or 'crossover' control P4 fully anticlockwise.
4. With a control input of -9V the heat output should be approximately 5 volts As the control input is reduced the heat output should reduce gradually to zero and the cool output should then increase gradually from zero to approximately 2 volts as the control input is reduced to -4V.
5. Set the control input to give approximately zero output on both channels. Check that there is no deadband between the heat and cool channels. Turn the overlap control P4 fully clockwise and check that simultaneous readings of approximately .25 volt can be obtained on both channels. Reset P4 fully clockwise.
6. Turn the 'relative bandwidth' control P1 clockwise and check that the cool output increases smoothly to approximately 1.5 volts. Turn P1 anticlockwise and check that the heat output increases smoothly to approximately 1.5 volts Reset P1 to its mid position.
7. Open circuit controller input and check that the cool output increases to approximately 5 volts after a short delay.
8. If no output is obtained from either channel, first check the continuity of the output winding then check the peak rectifying components D2, C9 or D3 C10 as appropriate. Check that the voltage across the appropriate oscillator smoothing capacitor C3 or C4 varies as the input signal is varied. Check that the oscillator is functioning mormally. The d.c. voltage table will assist in locating any fault.

D.C. Voltage Table.

Typical d.c. test voltages for the transistors are given in the table. With the output board and the main amplifier board inserted in the mother Board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input. Set the relative bandwidth' control P1 to its mid position and the 'overlap' or 'crossover' control P4 fully clockwise.

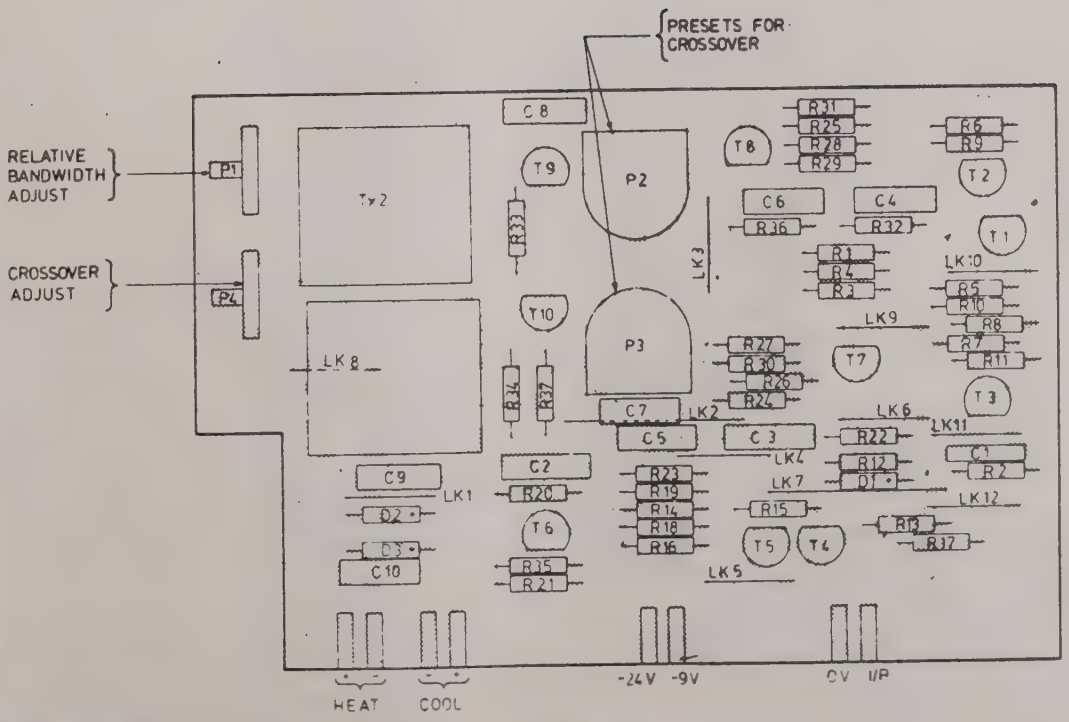
	CONTROL INPUT	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
EMITTER	-4V -9V	-3.6V -6 V	-3.6V -6 V	0 V 0 V	-6.8V -9.2V	-6.8V -9.2V	0 V 0 V	- 6.7V - 6.7V	- 4.8V - 4.8V	-4.8V -4.8V	-6.7V -6.7V
BASE	-4V -9V	-3 V* -5.4V*	-3 V* -5.4V*	- .6V - .6V	-6.2V* -8.6V*	-6.2V* -8.6V*	- .6V - .6V			-5.3V* -5.3V*	-6.1V* -6.1V*
COLLECTOR	-4V -9V	- .6V - .6V	0 V 0 V	- 3.8V -11 V	- .6V - .6V	0 V 0 V	- 2.9V -11 V	- 3.9V -11 V	- 2.9V -11 V	-6.7V -6.7V	- .3V - .3V

* Must be measured with an oscillope or electronic voltmeter due to high circuit resistance. All other measurements may be taken with a d.c. voltmeter having a resistance of 20KΩ/Volt. All voltages measured with reference to OV.



LILLIPUT MkII
DUAL 5v OUTPUT.

Drg Nº E92111 Sht 17



Drg No D93254.

Circuit no E92111 Sht 17

LILLIPUT Mk 2
DUAL 5V OUTPUT

ISOLATED 5 VOLT OUTPUT BOARD. (008/009)

Function

The 5 volt output board converts a 0 to 5 volt d.c. input into an electrically isolated 0 to 5 volt d.c. output with a current rating of 0.25mA.

Circuit Description

The input control signal operates between the levels -4V and -9V. The board is able to operate in two modes, normal or inverted, by changing links on the printed circuit board. In the normal mode, intended for heating applications, a control input of -4V corresponds to zero output and a control input of -9V corresponds to 5 volt output. In the inverted mode, intended for cooling applications where the output board is used in the parent controller, a control input of -4V corresponds to 4.5 volts output and a control input of -8.5V corresponds to zero output. The output is proportional to the input over the working range. The oscillator consisting of T3 TX1 and associated components derives its supply from the emitter followers T1, T2. The oscillator supply appears across the smoothing capacitor C2 and the peak value of the oscillation is only slightly less than the voltage across C2.(The peak to peak voltage is twice this value.) The secondary winding has a few more turns than the primary to allow for the forward voltage drop across diode D1. The peak rectifying and smoothing circuit D1, C5 thus produces an output voltage which is nearly equal to the voltage across C2. Transistor T3 is biased into conduction by the current through R8, the base drive being proportional to the oscillator supply voltage across C2. Positive feedback to T3 base via C4, R9 and the bias winding of TX1 causes the circuit to oscillate. The frequency of oscillation is fixed at approximately 30KHz by the parallel tuned circuit consisting of C3 and the primary inductance of TX1. The oscillation is sinusoidal. Resistor R10 provides base drive to T3 when the voltage across it is small ensuring that oscillation commences at very low applied voltages. Resistor R7 limits T3 peak collector current and ensures sinusoidal oscillation.

Normal Mode

The emitter potential of T2 is fixed at approximately -4V by the potential divider R3, R4. The emitter potential of T1 follows the input control signal and varies between -4.5V and -9.5V as the input signal is varied between -4V and -9V. The oscillation supply across C2 thus varies between 0.5 volt and 5.5 volts as the input signal is varied between -4V and -9V. Since the primary and secondary voltages are equal and the volt drop across D1 is 0.5 volt, the d.c. output signal varies from zero to 5 volts as the input signal is varied from -4V to -9V.

Inverted Mode

The emitter potential of T1 is fixed at -9.5V by its base connection to the -9V supply. The emitter potential of T2 follows the input control signal and varies between -4.5V and -9.5V as the input signal is varied between -4V and -9V. The oscillator supply across C2 thus varies between 5 volts and zero as the input signal is varied between -4V and -9V. Since the primary and secondary voltages are equal and the volt drop across D1 is 0.5 volt the d.c. output signal varies from 4.5 volts to zero as the input signal varied from -4V to 8.5V.

Checking

1. With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -4V, -9V and -28V supplies Failure of a power supply could be due to a fault on the mother board or the amplifier board.
2. Connect a 10V d.c. voltmeter between the control input and OV terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board. Place a 22KΩ resistor across the output.
3. If the board is connected in the normal mode set the control input to -9V and check that a 5 volt output, of the correct polarity, is obtained at the output. Gradually reduce the input control signal to -4V and check that the output reduces proportionally to within .3volt of zero output. If the output does not reduce sufficiently shunt R3 with an appropriate resistor in the space provided on the printed circuit board.
4. If the board is connected in the inverted mode set the control input to -4V and check that a 4.5 volt output, of the correct polarity, is obtained at the output. Gradually increase in the input control signal to 8.5V and check that the output reduces proportionally to zero.
5. If no output is obtained, first check C5, D1 and the continuity of the output winding. Check that the voltage across C2 varies between approximately zero and 5 volt as the input signal is varied and then check the oscillator. If the output is not controllable, first check that a variable voltage is obtained across C2 as the input signal is varied. The d.c. voltage table will assist in locating the fault. Note that due to the low value of R7 a fault on T3 may affect the previous stages.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are given in the table. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

NORMAL MODE

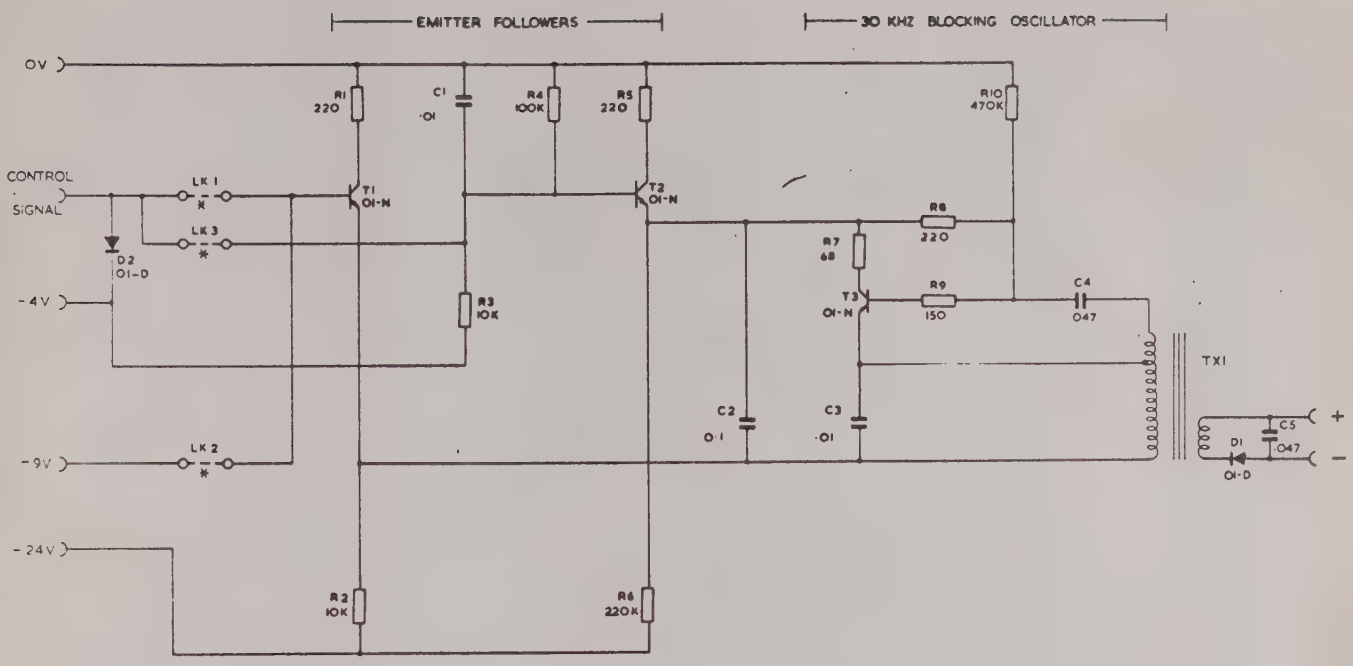
	CONTROL INPUT	T1	T2	T3
EMITTER	-4V -9V	-4.5V -9.5V	-3.8V -3.8V	-4.5V -9.5V
BASE	-4V -9V	-4V -9V	-3V -3V	-4V* -9V*
COLLECTOR	-4V -9V	-.5V -.4V	OV OV	-3.8V -3.8V

INVERTED MODE

	CONTROL INPUT	T1	T2	T3
EMITTER	-4V -9V	-9.5V -9.5V	-4.5V -9.5V	-9.5V -9.5V
BASE	-4V -9V	-9V -.3V	-4V OV	-9V* -9V*
COLLECTOR	-4V -9V	-.4V -.3V	OV OV	-4.5V -9.5V

All voltages measured with reference to OV with a 10d.c. voltmeter having a resistance of 20KΩ/volt.

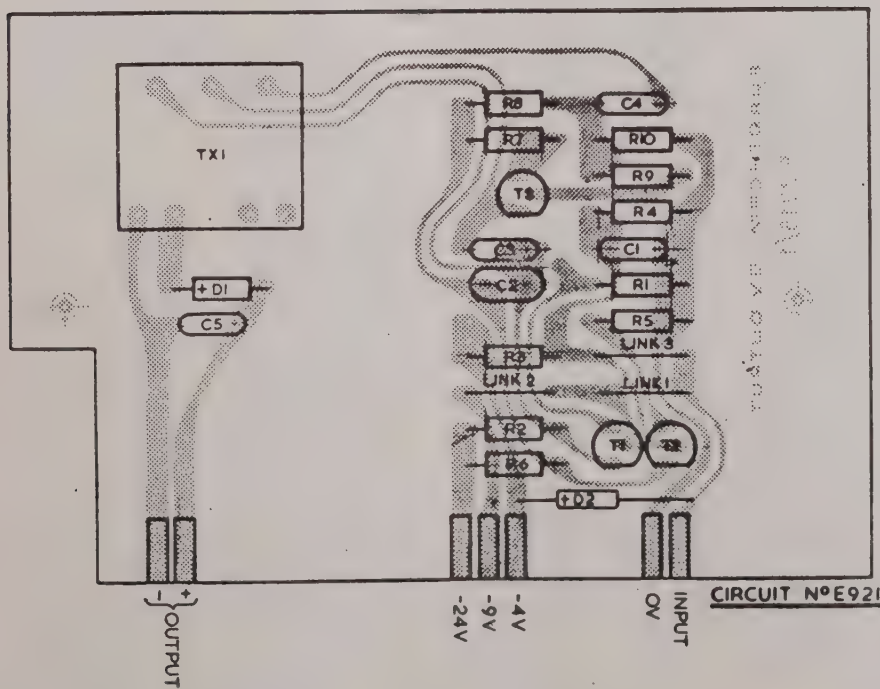
* Voltmeter current at this point may cause the oscillation to cease.



LINKS MARKED * VARY WITH MODE OF OPERATION.
REFER TO WRITE UP FOR DETAILS
LAYOUT Nº D93255

LILLIPUT Mk II.
ISOLATED 5V OUTPUT.

RG Nº E92111 Sht 16.



CIRCUIT Nº E92111 Sht 16

1. FOR NORMAL HEAT OPERATION LK1 IS MADE & LKS 2 & 3 OMITTED.
2. FOR INVERTED OUTPUT (COOL) LINK 1 OMITTED. LINK 2 MADE. LINK 3 MADE.

LILLIPUT Mk II
ISOLATED 5V OUTPU

Dng Nº D93255.

DUAL RELAY HEAT/COOL OUTPUT BOARD (023)

Function.

To allow slow cycling cooling and heating to be performed (simultaneously) whilst retaining three term control of the complete temperature control loop.

Both heating and cooling are ways of altering the heat input to a load. Cooling is negative heat input. It is desirable to ensure that the heating and cooling characteristics are both linear and as similar as possible with respect to heat transfer time constants in order to avoid loop stability problems. It is also advisable to ensure that the transition from heating to cooling as the input control signal is varied is as smooth as possible. Since in many cases the maximum cooling power provided is in excess of the maximum heating power some degree of gain alteration in either one or both channels will be required in order to ensure that the cooling characteristic of the controller will be the same as the heating characteristic.

The board consists of two slow cycling (time proportioning) relay stages either of which may be run in the synchronised (constant ON + OFF) or non-synchronised (variable period, variable ON time) mode. Normally the cooling channel will be synchronised and the heating channel will be free running. The input to the board is derived from the three term output of the amplifier board, which lies between -2V and -8.5V, -8.5V corresponds to maximum heating, -2V corresponds to maximum cooling and normally -6V corresponds to both zero heating and cooling. The heating channel is arranged so that for maximum heating the relay is ON all the time. The cooling channel is arranged so that for maximum cool input, the ON time may be varied over a fixed range thus effectively varying the gain in the cooling channel and enabling the heating and cooling regions to have the same sensitivity. As a result the cooling may never go to full ON in many systems.

Once the cooling gain has been correctly adjusted, a linear power control characteristic is produced which remains linear as the proportional band of the complete controller is adjusted.

When the characteristic is adjusted to be linear the maximum heating power occurs with a change of input signal of 2.5V. The slope of the line is thus $P_H/2.5$ watts/Volt. Due to the limitations of the drive circuit only 4V are available for the cooling region, thus the maximum cooling power allowed by the unit must be given by $P_C = 1.6P_H$.

Effect of Non-linearity in Cooling and Heating

It is not unusual for both the heating and cooling units to have a certain amount of non-linearity at very small relay closure time due to valve imperfections etc. In this event the overall characteristic will be rather non-linear. This can be overcome by application of the correct amount of cross-over which has the effect of moving the heating and cooling characteristics so that heating commences slightly in the cooling region whilse cooling commences slightly in the heating region.

A small region therefore exists where both heating and cooling systems are in operation simultaneously. The non-linearity can thereby be much decreased, however the crossover must be the minimum possible and applied with care as it can otherwise increase both the non-linearity and the gain in the centre region and make satisfactory operation more difficult.

CIRCUIT DESCRIPTION

Heating Circuit

A hysteretic switch is produced by transistors T_{10}, T_{11} and T_{12} with switching points at T_{10} base defined by R_{33}, R_{34}, R_{32}, R_{36}, R_{42} and the supply lines at approximately -0.9V and 2.4V. T_8 and T_9 form an integrator with integrating capacitor C_3. The input to the circuit is applied via R_{24} and the feedback current to the integrator is produced by T_{13} acting through R_{29} and P_5. When T_{13} is ON so also is T_{14} and the heating relay is then energised. The voltage applied to the combination R_{29} and P_5 varies dependent on whether T_{13} is ON or OFF, when T_{13} is ON it is at 14V and the integrator output moves in such a direction as to try to turn T_{13} off via the hysteretic switch circuit. When T_{13} is OFF the junction of D_3 and R_{38} is at approximately -9V (defined by D_3 and D_5 whose forward drop voltages are arranged to oppose). The integrator output then moves in such a direction as to try to turn T_{13} ON again. An oscillation is therefore set up in which the ON time of T_{13} varies with the input voltage, increasing as the input voltage goes more negative. Potentiometer P_4 enables the circuit to be adjusted to be fully on for the appropriate input voltage since in the ON state no current flows in R_{29}. Potentiometer P_5 enables zero heating to be set. The oscillation frequency is mainly controlled by the integral capacitor and the resistors feeding the integrator input.

Cool Circuit

This functions in a similar way to the heating circuit but there are detail differences. T_4, T_5 and T_6 form the hysteretic switch circuit with switching points defined by the supply lines together with the resistors R_{10}, R_{13}, R_{16}, R_{17}, R_{18}, R_{19} and R_{20}. The switch is driven by transistors T_2 and T_3 which form an integrator circuit with C_1 as the integrating capacitor. The switching points of the hysteretic switch are approximately -5.9V and -9.6V at the negative end of C_1, the integrator output. The potential at the junction of R_{19} and R_{20} is used to drive transistor T_1 which is either cut off completely when T_6 is cut off and the junction point of R_{19} and R_{20} is at approximately -9V, or passes a current given by 3V across R_{50} and P_3 when the R_{19}, R_{20} junction goes to -5.4V as T_6 turns on. A square wave of current flows into the integrating capacitor and an oscillation is set up in the circuit in which the ON to OFF time of T_1 is governed by the necessity for the average current in T_1 to equal the net input current into the integrator virtual earth point from all other sources, i.e. R_1, R_6 and R_7. When T_1 is conducting T_7 will also be conducting and the cool relay energised. The ON time over the cooling relay is therefore controlled by both the input voltage, increasing as the input signal becomes less negative, and by the resistance in the emitter of T_1, increasing as this increases in value. The frequency of this oscillation is a function of the integrating capacitor and of the emitter resistor of T_1. Potentiometer P_2, enables the cooling ON time to be set to zero at the appropriate input voltage and potentiometer P_3 allows the ON time at any input voltage to be adjusted.

Synchronising Oscillator

T_{16} and T_{17} form a type of multivibrator in which the mark to space ratio can be made inherently very close to unity and which uses only one timing capacitor. The transistor pair has positive feedback via C_7 such that there are only two states of the system, either T_{16} conducting and T_{17} off or visa versa. Neither state is astable as when T_{16} is conducting the current in R_{46} charges C_7 and eventually forces the emitter of T_{17} more negative than its base so that conduction commences and the circuit switches state. The base of T_{16} is then driven more negative than its emitter which is held (momentarily) by C_7 and T_{16} cuts off. The current in R_{45} then charges C_7 and eventually carries the emitter of T_{16} more negative than its base, turning T_{16} ON again. Positive feedback then cuts T_{17} OFF and the base - emitter junction of T_{16} carries C_7 positively since the emitter of T_{17} now no longer has control. The positive end of C_7 is now held fixed by T_{16} emitter and the cycle begins again. The period of the complete cycle is approximately $4C_7R_{44}$ seconds and provided the voltage across R_{46} and R_{45} is large compared with the change of voltage across R_{44} the mark to space ratio will be close to unity. Synchronisation of the heat and cool relay circuits is produced by differentiating the square wave appearing across R_{44} by means of C_5 and C_6 and applying the resulting short pulses to the hysteretic switches. When synchronisation is not required the appropriate capacitor is omitted.

Crossover Circuit

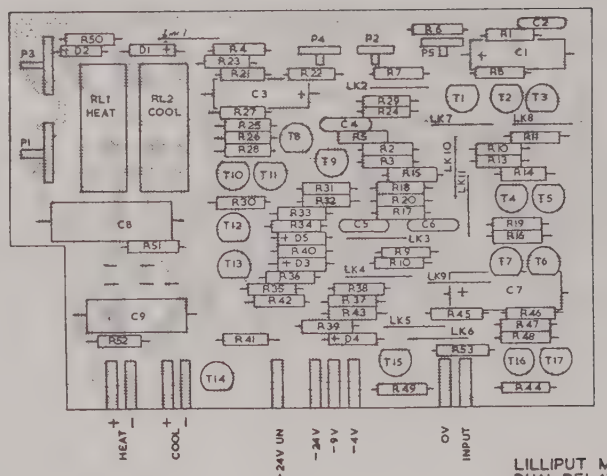
When P_1 is short circuited no current flows in the resistors R_6 and R_{23} so that at the appropriate input voltage corresponding to zero heating and zero cooling when these two circuits are correctly set up neither the heat nor the cool relay will operate. If P_1 is now set to maximum resistance two approximately equal and opposite voltages (0.5V) appear at its ends relative to the -4V line. These are applied to the heat and the cool circuits in such a way as to make them begin cycling. The effect is thus a zero shift in opposite directions of equal amounts to both the heating and cooling circuits so that a region in generated where both the heating circuit and the cooling circuit are operating. The extent of this region varies with the setting of P_3.

Power Supplies

The board is supplied with the normal -9V, -4V and -24V lines. The -9V and -24V lines are used directly whilst the -4V line is buffered by T_{15} to enable the loading imposed on this line by the circuit to be withstood. The base emitter voltage at T_{15} is approximately equal to the diode voltage drop in D_4 and varies similarly with temperature so that the buffered -4V line remains relatively stable. Resistor R_{39} supplies the majority of the current loading on the -9V line so that the instrument stabilised supplies are unaffected by the insertion of the relatively high loading of this board.

External Connections

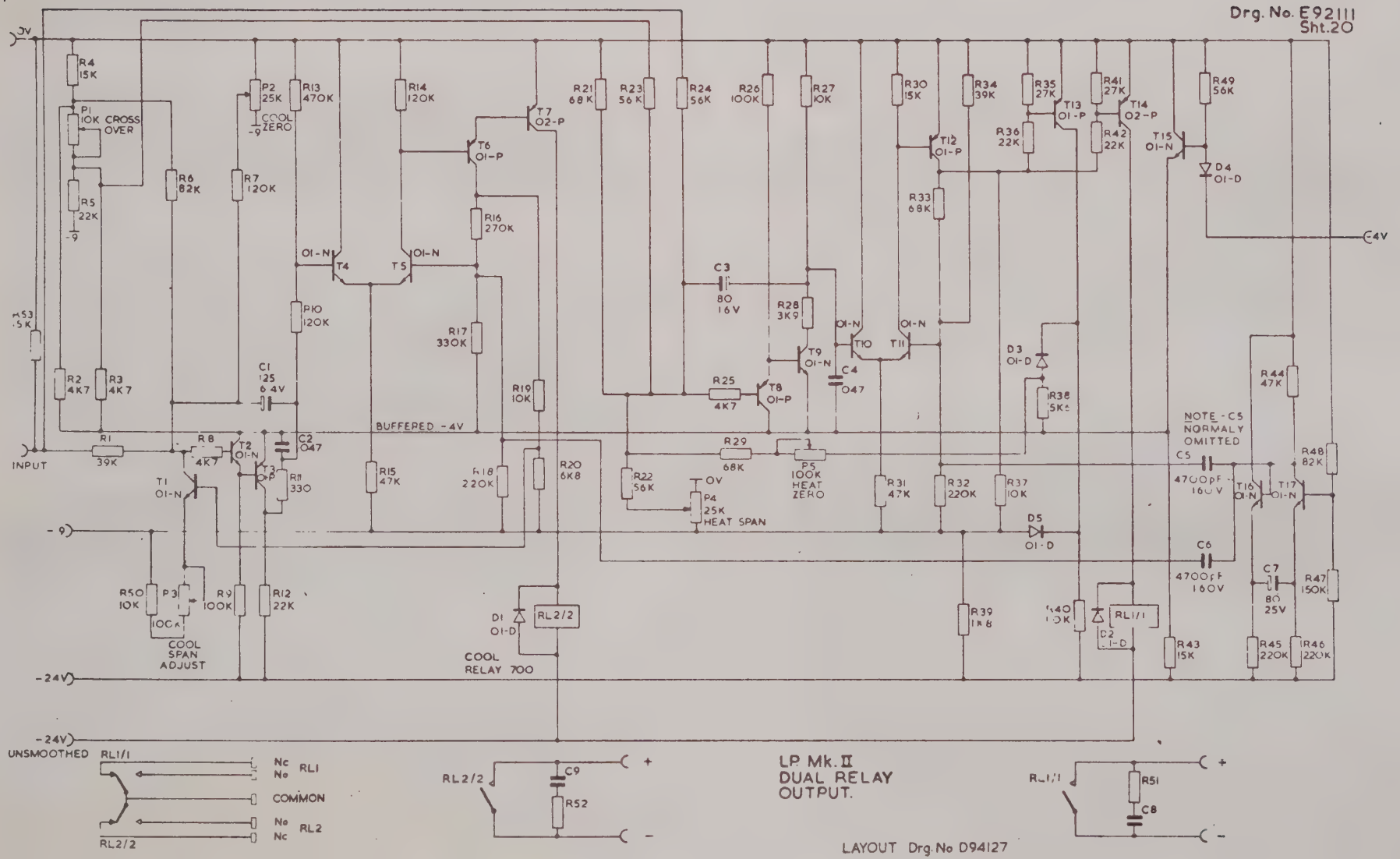
One pair of normally open contacts from each relay is brought out via the mother board pins to the rear of the instrument. Spark suppression circuitry is fitted across these contacts on the printed circuit board. The second pair of changeover contacts from each relay is brought out to "Amp" pins on the printed circuit board to enable indication of the relay states.



LILLIPUT Mk II
DUAL RELAY OUTPUT

Drg No D 94127

Circuit No F 2111 Sht 20.


Drg. No. E92111 Sht.20
0V
-9
-24V
INPUT
BUFFERED -4V
+4V
R4 15K
P1 10K CROSS OVER
R5 22K
R6 82K
P2 25K COOL ZERO
R7 120K
R13 470K
R14 120K
R16 270K
P10 120K
R17 330K
R19 10K
R53 15K
R2 4K7
R3 4K7
C1 125 6.4V
R1 39K
R8 4K7
T2 01-N
C2 047
T3 01-P
R11 330
T1 01-N
R15 47K
R18 220K
R20 6K8
T4 01-N
T5 01-N
T6 01-P
T7 02-P
R21 68K
R23 56K
R24 56K
R26 100K
R27 10K
C3 80 16V
R28 3K9
R25 4K7
T8 01-P
T9 01-N
T10 01-N
T11 01-N
C4 047
R29 68K
P5 100K HEAT ZERO
R22 56K
P4 25K HEAT SPAN
R31 4.7K
R32 220K
R37 10K
R30 15K
T12 01-P
R33 68K
R34 39K
R35 27K
T13 01-P
R36 22K
R41 27K
T14 02-P
R42 22K
T15 01-N
R49 56K
D4 01-D
D3 01-D
R38 5K6
D5 01-D
R44 47K
NOTE - C5 NORMALLY OMITTED
C5 4700pF 160V
T16 01-N
T17 01-N
R48 82K
C6 4700pF 160V
C7 80 25V
R47 150K
R50 10K
P3 10K
R9 100K
R12 22K
COOL SPAN ADJUST
D1 01-D
RL2/2
COOL RELAY 700
R39 1K8
R40 10K
D2 01-D
RL1/1
R43 15K
R45 220K
R46 220K
UNSMOOTHED
RL1/1
Nc
No
RL1
COMMON
No
Nc
RL2
RL2/2
RL2/2
C9
R52
+
-
RL1/1
R51
C8
+
-
LP. Mk. II
DUAL RELAY
OUTPUT.
LAYOUT Drg. No D94127

ISOLATED MILLIAMP OUTPUT BOARD (067 - 073)

Function

The isolated milliamp output converts a 0 to 5 volt d.c. input into an electrically isolated 0 to 10mA (20V) current output or a 0 to 20mA (12V) current output or a 0 to 5V (10mA) voltage output.

Circuit Description.

The input control signal operates between the levels -4V and -8.2V. For normal operation links 12 and 13 are made and inputs of -4V and -8.2V correspond respectively to minimum and maximum output. By making links 11 and 14 instead of links 12 and 13 an inverted operating mode is achieved where inputs of -4V and -8.2V correspond respectively to maximum and minimum output. Output of 0 to 5V, 0 to 10mA or 0 to 20mA in either mode are achieved by suitable selection of R31, R34, LK1, LK2, LK3, LK4 as indicated on the circuit diagram. Outputs of 1 to 5V, 2 to 10mA or 4 to 20mA are achieved by suitable selection of R3, R4, R5 as indicated on the circuit diagram.

The input control signal is fed via emitter-followers T1 and T2 into the control oscillator consisting of T3, TX1 and associated components. The control oscillator produces an isolated d.c. voltage across C4 which is proportional to the input control signal. In the normal mode a -4V control input corresponds to minimum voltage across C4 (zero or 1 volt depending on output range) and an input voltage of -8.2V corresponds to 5 volts across C4. The buffer amplifier T8 to T10 and associated components converts the 0 to 5 volt (or 1 to 5 volt) signal across C4 into a 0 to 10mA (or 2 to 10mA) current signal with an output voltage capability of 20 volts. Current outputs of 0 to 20mA or 4 to 20mA with an output voltage capability in excess of 12 volts can also be provided by suitable component selection. Alternatively the 0 to 5 volt (or 1 to 5 volt) signal across C4, which has a current capability of only 0.25mA, can be converted to a 0 to 5 volt (or 1 to 5 volt) signal with an output current capability of 10mA. To give complete output isolation an isolated 28 volt buffer supply is provided via a d.c. to d.c. converter consisting of transistors T4 to T7, transformer TX2, diodes D4 to D7 and associated components. Network C9, R24, D8 provides smoothing of the isolated 28V buffer supply without direct capacitive loading of the converter, since direct capacitive loading could cause the converter action to cease. Resistor R24 provides a suitable charging impedance for C9 and diode D8 provides a low impedance discharge path to maintain the buffer supply whilst the converter switches at the end of each half cycle. Resistor R27 provides h.f. interference rejection. Components C10, C11, R30 provide h.f. feedback stabilisation for amplifier T1, T2. Resistors R32, R33 are h.f. stoppers and resistor R34 provides output short circuit protection when the output is 0 to 5 volts. Diode D9 protects T10 from excessive forward voltage when the current output is used to drive an inductive load.

Control Oscillator.

The control oscillator consisting of T3, TX1 and associated components is biased into conduction by current through R11, giving base drive to T3 which is proportional to the oscillator supply voltage across C1. Positive feedback to T3 base via C3, R12 and the bias winding of TX1 causes the circuit to oscillate sinusoidally at a frequency of 30KHz defined by the parallel tuned circuit consisting of C2 and the primary inductance of TX1. Resistor R13 provides base drive to T3 when the voltage across C1 is small, ensuring that oscillation commences at very low applied voltage. Resistor R10 limits T3 peak collector current and ensures sinusoidal oscillation. The peak value of oscillation on the primary of TX1 is only slightly less than the oscillator supply voltage across C1 (the peak to peak voltage is twice this value). The secondary winding has a few more turns than the primary winding so that the voltage across C4 is equal to the input voltage.

Supply Converter.

The self-oscillating d.c. to d.c. converter consisting of transistors T4 to T7, transformer TX2 and associated components provides a 4KHz square wave of peak to peak amplitude 28 volts across the primary of TX2. A square wave of peak to peak amplitude 70 volts is reflected in the secondary winding of TX2, providing an isolated d.c. supply of approximately 32 volts via diodes D4 to D7. At maximum loading of 20mA the isolated supply voltage falls to approximately 24 volts due to regulation of the -28V instrument supply and regulation of the converter. The converter consists essentially of transistors T4 and T7, transformer TX2 and capacitors C7 and C8. One side of TX2 primary is held at -14V by voltage sharing capacitors C7, C8, and the other side of TX2 primary is switched alternately between 0V and -28V due to alternate conduction of T4 and T7. Voltage sharing capacitors are used to ensure that no d.c. component is present in the primary current of TX2. When T4 conducts, positive feedback to T4 base via R17 and the primary bias winding ensures that T4 remains hard 'on' and T7 remains 'off'. When T17 conducts, positive feedback to T7 base via C5, R20 ensures that T7 remains hard 'on' and T4 remains 'off'.

In the absence of T5, T6 the 'on' time of transistors T4 and T7 would be determined by the saturation time of the transformer core. Transistors T5, T6 are included to drive the converter at a higher frequency than would result from saturation commutation, thereby avoiding excessive peak currents in transistors T4 and T7 at the end of each half cycle. The frequency of oscillation is fixed at 4KHz by capacitor C6 in association with resistors R15, R16, R18. When T4 conducts the common emitters of T4, T7 rise to 0V and the bias winding gives a +3.5V supply at junction R17, C5. Transistor T4 is thus held hard 'on' by base current through R17 and transistor T7 is held 'off'. Junction C6, R18 rises initially to +7.5V due to the 4 volt charge acquired on C6 during the previous half cycle, thus holding transistor T5'of'. Capacitor C6 recharges via R15, R18 until junction C6, R18 falls to a potential of -0.5V, at which point T5 begins to conduct and the drive to T4 base is removed. When conduction in T4 ceases, the primary voltage of TX2 reverses and positive

feedback to T7 base via the bias winding and C5, R20 ensures that T7 is driven hard 'on', thus applying -28V to the primary winding of TX2. Junction C6, R18 falls initially to -35.5V and T7 remains 'on' until C6 recharges to -27.5V via R16, R18, at which point conduction of T6 removes the base drive to T7 and the cycle repeats continually. Unity mark to space ratio is achieved by providing equal charge and discharge paths for C6 via R15, R18 and R16, R18. Unity mark to space ratio in conjunction with the decoupling action of C7, C8 ensures positive and negative half cycles of equal magnitude and duration. Components C5, R19, R23 are included to ensure satisfactory self-starting of the converter by biasing T4 into conduction when the supply voltage is connected. Diode D3 prevents charging of C5 due to rectification at T7 base and thereby ensures that full drive is applied to T7 via R20 during negative half cycle. Resistors R21 and R22 are h.f. stoppers which also provide a degree of current-limit protection for T4 and T7 during start-up. Resistor R14 prevents converter current from circulating through the instrument power supplies, the primary current for TX2 being drawn from C7 when T4 conducts and from C8 when T7 conducts. For all normal uses the two secondary windings of TX2 are connected in series by making links 5 and 8. This gives an isolated d.c. supply voltage of approximately 24 volts at maximum loading of 20mA. By making links 6 and 8 instead of links 5 and 8 a 0 to 50mA (6V max.) current output can be provided.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are given in the table for operation in the normal mode with a 0 to 10mA output. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

NORMAL MODE WITH 0 to 10mA OUTPUT

	CONTROL INPUT	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
EMITTER	-4V	-4.6V	-.2V	- 5.3V	-14 V	-14.5V	-14 V	-14 V	+ .6V	0 V	0 V
	-9V	-9.3V	-4.8V	-10 V	-13.5V	-13.5V	-13.5V	-13.5V	+ .6V	0 V	+1.5V
BASE	-4V	-4 V	-4 V	- 4.7V*	-14.5V	-14.5V	-14.5V	-14 V	0 V	+ .6V	0 V
	-9V	-8.5V	-4 V	- 9.7V*	-13.5V	-12.5V	-12.5V	-13.5V	0 V	+ .6V	+2.1V
COLLECTOR	-4V	- .3V	- .1V	- 5 V	- .1V	-14 V	-14 V	-28 V	0 V	0 V	+32 V
	-9V	- .2V	- .1V	- 5 V	- .3V	-13.5V	-13.5V	-27 V	0 V	+2.2V	+28 V

All voltages measured with a d.c. voltmeter having a resistance of 20Kohm/volt
All voltages measured with reference to OV, except for T8, T9, T10 whose voltages are measured with reference to T8 collector. The output load was a short circuit.

* Voltmeter current at this point may cause the oscillation to cease.

1. With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -4V, -9V and -28V supplies. Failure of a power supply could be due to a fault on the mother board or the amplifier board.

2. Connect a 10V d.c. voltmeter between the control input and OV terminals on the output board. Demand full power from the controller and check that the input signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.

3. Check the board as follows depending on the type of output.

0 to 10mA or 2 to 10mA output

Place a 1.8Kohm resistor and a 10mA d.c. meter in series across the output terminals. If the board is connected in the normal mode check that the output increases gradually from 0 to 10mA (or from 2 to 10mA) as the control input is increased from -4V to -9V. If the board is connected in the inverted mode check that the output increases gradually from 0 to 10mA (or 2 to 10mA) as the control input is reduced from -9V to -4V.

0 to 20mA or 4 to 20mA output

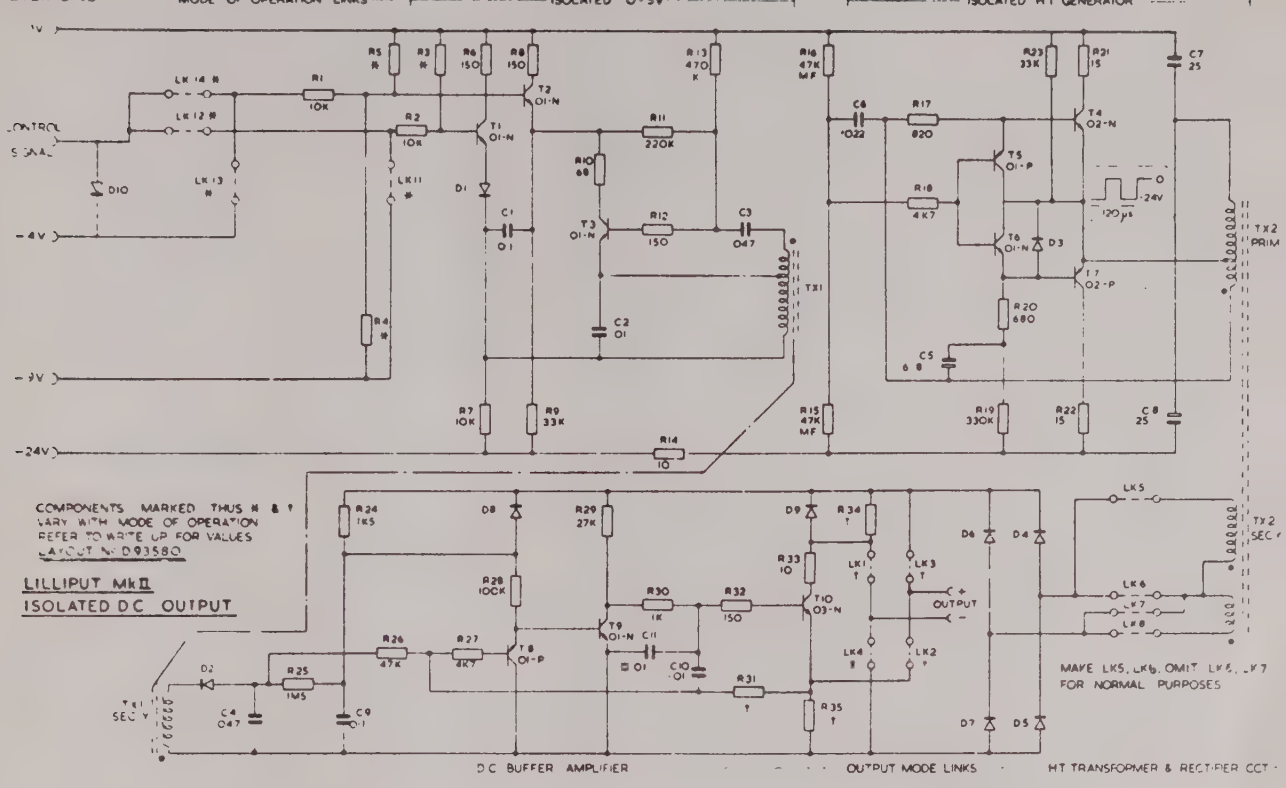
Place a 680ohm resistor and a 20mA d.c. meter in series across the output terminals. If the board is connected in the normal mode check that the output increases gradually from 0 to 20mA (or from 4 to 20mA) as the control input is increased from -4V to -9V. If the board is connected in the inverted mode check that the output increases gradually from 0 to 20mA (or 4 to 20mA) as the control input is reduced from -9V to -4V.

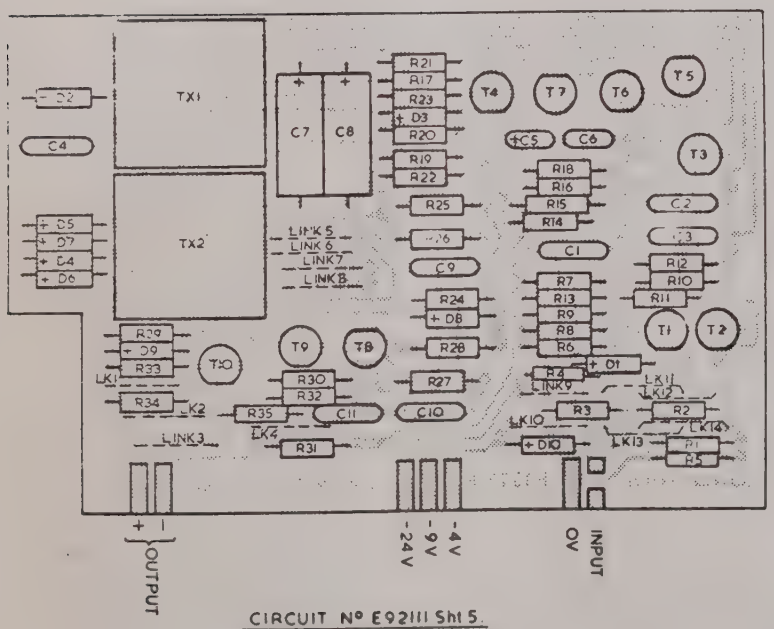
0 to 5 volt or 1 to 5 volt output

Place a 470 ohm resistor and a 10V d.c. voltmeter in parallel across the output terminals. If the board is connected in the normal mode check that the output increases gradually from 0 to 5 volt (or from 1 to 5 volts) as the control input is increased from -4V to -9V. If the board is connected in the inverted mode check that the output increases gradually from 0 to 5 volts (or 1 to 5 volts) as the control input is reduced from -9V to -4V.

4. If no output is obtained first check the isolated 28 volt buffer supply between D7 anode (-) and D6 cathode (+). This should be between 22 volts and 36 volts depending on the output load and mains voltage. If this supply is present next check that the voltage across C1 varies between approximately .5 volt and 5.5 volts as the input signal is varied between -4V and -9V. Check that the voltage at junction C4, R26 varies between zero and -5 volts, with reference to T8 collector, as the input signal is varied between -4V and -9V. If the board is connected for current output, check that the voltage at junction R31, R35 varies between zero and +1.5 volts, with reference to T8 collector, as the input signal is varied between -4V and -9V. If the board is connected for 5 volt output, check that the voltage at junction R31, R35 varies between zero and +5 volts, with reference to T8 collector, as the input signal is varied between -4V and -9V. The d.c. voltage table will assist in locating any fault.

E92111 Sht 5





CIRCUIT No E92111 Sht 5.

INPUT	Lnk11	Lnk12	Lnk13	Lnk14	R3	R4	R5
0-100%	—	✓	✓	—	—	120K	—
20-100%	—	✓	✓	—	39K	—	68K
100-0%	✓	—	—	✓	220K	—	—
100-20%	✓	—	—	✓	68K	—	39K

OUTPUT	Lnk1	Lnk 2	Lnk 3	Lnk 4	R31	R34	R35
10mA. Max	✓	—	✓	—	15K	—	150
20mA "	✓	—	✓	—	15K	—	75
5V "	—	✓	—	✓	56K	820	1K
10V "	—	✓	—	✓	120K	560	22K

Drg No D93580

LILLIPUT Mk II,
ISOLATED D.C. OUTPUT.

HIGH/LOW LIMIT (Options 02/03)

Function

The limits circuit provides operation of a relay at adjustable temperatures above or below the set point. High limit operation occurs at temperatures above the set point and low limit operates below the set point. The limits are adjustable between 0 and 10% of span.

Circuit Description

The output from the error amplifier is applied to the input of the positive gain feedback amplifier formed by transistors T1 to T3 and associated components. The output signal from this amplifier, taken from the junction of R6, R7 is applied to the hysteretic switching circuits formed by transistors T4, T7 and T5. The relay RL1 is normally energised by conduction of T8. When the amplifier output reaches a level corresponding to either limit, as defined by P2 setting, hysteretic switching action causes T8 and the relay to switch off.

The amplifier consists of a differential pair input stage T1, T2 and a single ended output stage T3. Negative feedback from the output at R6, R7 junction to the inverting input at T2 base via R5, P1 controls the amplifier gain. Potentiometer P2 provides adjustment of the base bias on T6 or T7 in the high or low limit modes respectively and determines the limit setting.

For high limit operation, only links 3,5 and 6 are inserted and resistors R21, R22, R25, R26 are omitted. In the high limit mode, the amplifier output is fed to T4 base via R11 and link 6. With zero error input to T1 base when the load temperature is at the set point. T4 conducts by virtue of the greater negative bias on T7 base and supplies emitter current to the T5, T6 differential pair. Transistor T6 conducts and the relay is energised via D1 and T8.

As the load temperature increases towards the high limit, an increasing negative input is applied to T1 base. The amplifier output thus increases negatively and T4 conduction ceases as T4 base voltage increases negatively beyond T7 base voltage. The bias on T7 base is defined by the setting of potentiometer P2. As T4 is switched off, the emitter drive current to T5 T6 is removed and the relay is de-energised. In the high limit condition positive feedback is applied to T4 base from T7 collector via R14 which holds T4 firmly off. The switching pair T4, T7 next change state, causing the relay to energise, only when the amplifier output rises sufficiently positive to overcome the hysteresis thus applied.

For low limit operation, only links 2, 4 and 7 are inserted with resistors R18, R19, R27, R28 omitted. In the low limit mode, the amplifier output is fed to T5 base via R10 and link 2. With zero error input to T1 base, when the load temperature is at the set point, T5 is non-conducting by virtue of the greater positive base bias on T6 base which holds T6 on. Diode D1 therefore conducts and the relay is energised via T8. As the load temperature decreases towards the low limit, an increasing positive input is applied to T1 base. The amplifier output thus increases positively and T5 conducts as T5 base voltage increases positively beyond T6 base voltage, the latter being determined by P2 setting. Conduction of T5 causes the relay to de-energise as D1 and T8 Cut off. In the low limit condition, positive feedback is applied to T5 base from T6 collector via R13 which holds T5 firmly on. The switching pair T5, T6 next change state only when the amplifier output falls sufficiently negative to overcome the hysteresis thus applied.

Diode D2 protects T8 from inductive voltage spikes produced by the relay coil. The resistor chain R18 to R22 provides standing biasfor T6 and T7. This bias is modified by an additional current bleed from the limits potentiometer P2. Capacitor C1 provides smoothing of the amplifier output signal and capacitors C3, C4 provide high frequency interference rejection. Capacitor C2 stabilises the feedback amplifier.

If the relay contacts are required to be closed at the set point and open in the alarm condition, link 10 must be made and link 9 omitted.

If the relay contacts are required to be open at the set point and closed in the alarm condition, link 9 must be made and link 10 omitted.

Checking

1. With the limits board and the main amplifier board inserted in the mother board, connect the mains supply and check the -24V, -28V +24V, -4V and -9V supplies with a d.c. voltmeter. Failure of any of the power supplies could be due to a mother board fault.
2. Set the control temperature to a value approximately mid-span and inject a corresponding signal into the thermocouple input from a millivolt source. With zero error, ensure that the relay is energised.
3. Set the limit alarm potentiometer P2 to approximately mid way (5%) Note whether the board is connected for high or low limit. Slowly switch the injected millivolt signal to a value corresponding to 5% away from a set point towards the relevant limit. Ensure that the relay de-energises at the alarm point.
4. Return the injected signal to correspond to set point. Check that the relay re-energises.
5. Check the limit alarm operation at the two extreme settings of the limit potentiometer (1 and 10% of span) If the alarm is not functioning correctly check the operation of T1, T2 and T3 with reference to the d.c. voltage table. If no fault is indicated, check the operation of T4 to T8.

D.C. Voltage Table.

Typical d.c. test voltages for the transistors are shown in the table. All voltages are measured with reference to OV using a d.c. voltmeter having a resistance of 20K /Volt. The limit range control P1 must be set to approximately mid position and the limit control P2 must be set to the maximum fully clockwise position. Voltages are checked with the indicator upscale (maximum over temperature error) or downscale (maximum under temperature error) as appropriate and with the indicator at the set point, (zero error).

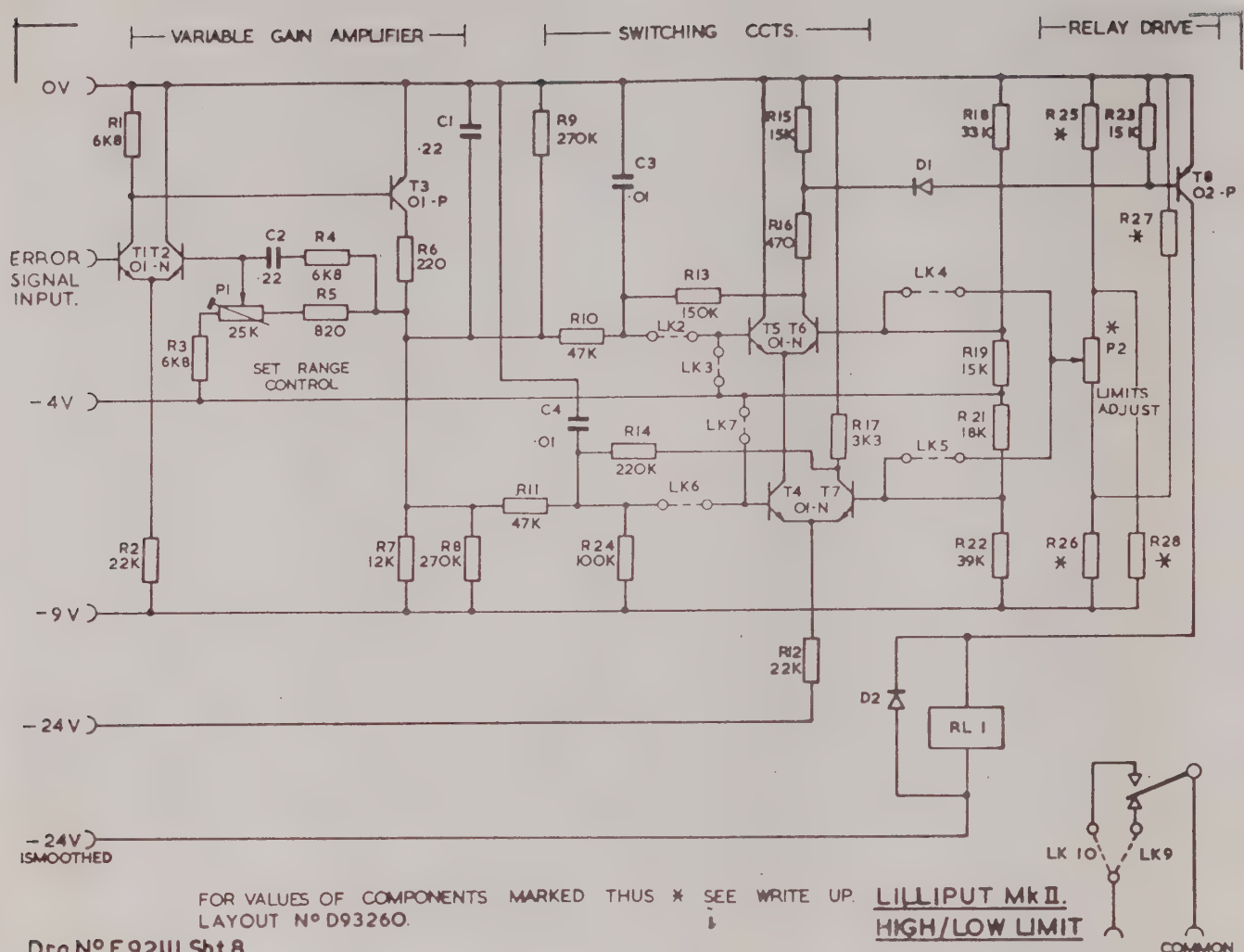
Low Limit Board.

	INDICATOR POSITION	T1	T2	T3	T4	T5	T6	T7	T8
EMITTER	Set Point (zero error)	-4.5	-4.5	0	-4.5	-2.5	-2.5	-4.5	0 V
	Downscale (max error)	-2.5	-2.5	0	-4.5	-1	-1	-4.5	0 V
BASE	Set Point	-4	-4	-0.5	-4	-3	-2	-5	-1 V
	Downscale	-2	-2	-0.5	-4	-0.5	-2	-5	0 V
COLLECTOR	Set Point	-0.5	0	-4	-2.5	0	-2	-ve	-ve V
	Downscale	-0.5	0	-0.5	-1	0	-ve	-ve	-20 V

Points designated only '-ve' are close to zero but slightly negative.

High Limit Board.

	INDICATOR POSITION	T1	T2	T3	T4	T5	T6	T7	T8
EMITTER	Upscale (max error)	-6.5	-6.5	0	-7	-ve	-ve	-7	0 V
	Set Point (zero error)	-4.5	-4.5	0	-5.5	-3.5	-3.5	-5.5	0 V
BASE	Upscale	-7	-6	0	-6	-4	-3	-6	0 V
	Set Point	-4	-4	-0.5	-4	-4	-3	-6	-1 V
COLLECTOR	Upscale	0	0	-7	-ve	0	-0.5	-3	-21V
	Set Point	-0.5	0	-4	-3.5	0	-2	-ve	-ve V



FOR VALUES OF COMPONENTS MARKED THUS * SEE WRITE UP. LAYOUT Nº D93260.

LILLIPUT Mk II. HIGH/LOW LIMIT

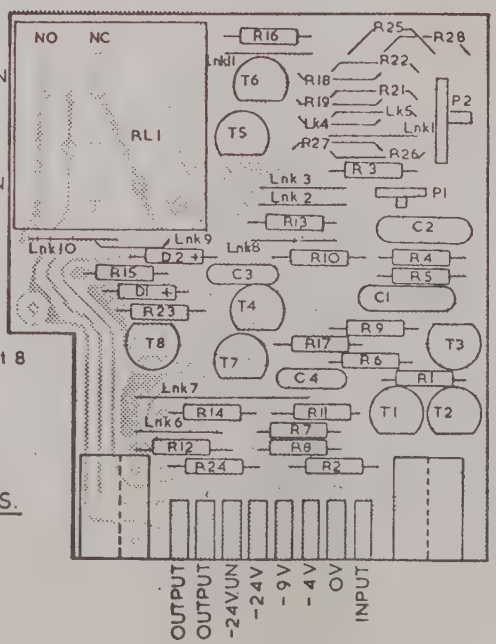
Drg Nº E92111 Sht 8

	R18	R19	R21	R22	R25	R26	R27	R28	P2	LINKS 2	3	4	5	6	7
HL	33K	15K	—	—	—	—	56K	27K	22K	–	✓	–	✓	✓	–
LL	—	—	18K	39K	22K	56K	—	—	22K	✓	–	✓	–	–	✓

CONTACTS CLOSING IN ALARM CONDITION
ADD LINK 9
OMIT LINK 10

CONTACTS OPENING IN ALARM CONDITION
ADD LINK 10
OMIT LINK 9.

CIRCUIT Nº E92111 Sht 8



LILLIPUT MkII. HIGH/LOW LIMITS.

Drg Nº D93260

ALL LIMITS BOARD. (Option 04)

Function

The limits circuit provides operation of a relay at adjustable temperatures equally above and below the set point. The limits are adjustable between 1 and 10% of span.

Circuit Description

The output from the error amplifier is applied to the input of the positive variable gain feedback amplifier formed by transistors T1 to T3 and associated components. The output signal from this amplifier, taken from the junction of R5, R6 is applied to the hysteretic switching circuits formed by transistors T4, T5 and T6, T7. The relay is normally energised by conduction of T8. When the amplifier output reaches a level corresponding to either limit, as defined by P1 setting, hysteretic switching action causes T8 to switch off and the relay to de-energise.

The amplifier consists of a differential pair input stage, T1, T2, and a single ended output stage T3. Negative feedback from the output at R5, R6 junction to the inverting input at T2 base via R3, P1 controls the amplifier gain. Potentiometer P1 provides adjustment of the limit setting.

With an error input of zero volts when the load temperature is at the set point, T6 conducts by virtue of the negative 1.5 volts bias on T7 base (with respect to -4 volts) provided by R20, R21 and supplies emitter current to the T4, T5 differential pair. Transistor T5 conducts by virtue of the +1.5 volt bias on T5 base (with respect to -4 volts) provided by R18, R19 and the relay is energised via D1, and T8.

As the load temperature increases towards the high limit, an increasing negative input is applied to T1 base. The amplifier output thus increases negatively and T6 conduction ceases as T6 base voltage increases negatively beyond T7 base voltage. As T6 is switched off, the emitter drive current to T4, T5 is removed and the relay is de-energised. In the high limit condition, positive feedback is applied to T6 base from T7 collector via R13 which holds T6 firmly off. The switching pair T6, T7 next change state, causing the relay to energise, only when the amplifier output rises sufficiently positive to overcome the hysteresis thus applied.

As the load temperature decreases towards the low limit, an increasing positive input is applied to T1 base. The amplifier output thus increases positively and T4 conducts as T4 base voltage increases positively beyond T5 base voltage. As conduction in T4 commences, T5 is switched off. Diode D1 therefore becomes non-conducting and T8 and the relay are switched off. In the low limit condition, positive feedback is applied to T4 base from T5 collector via R12 which holds T4 firmly on. The switching pair T4, T5 next change state, causing the relay to energise, only when the amplifier output falls sufficiently negative to overcome the hysteresis thus applied.

Diode D2 protects T8 from inductive voltage spikes produced by the relay coil. Capacitor C2 provides smoothing of the amplifier output signal and capacitors C3, C4 provide high frequency interference rejection.

Capacitor C1 stabilises the feedback amplifier.

If the relay contacts are required to be closed at the set-point and open in the alarm condition, link 2 must be made and link 3 omitted. If the relay contacts are required to be open at the set point and closed in the alarm condition, link 3 must be made and link 2 omitted.

Checking

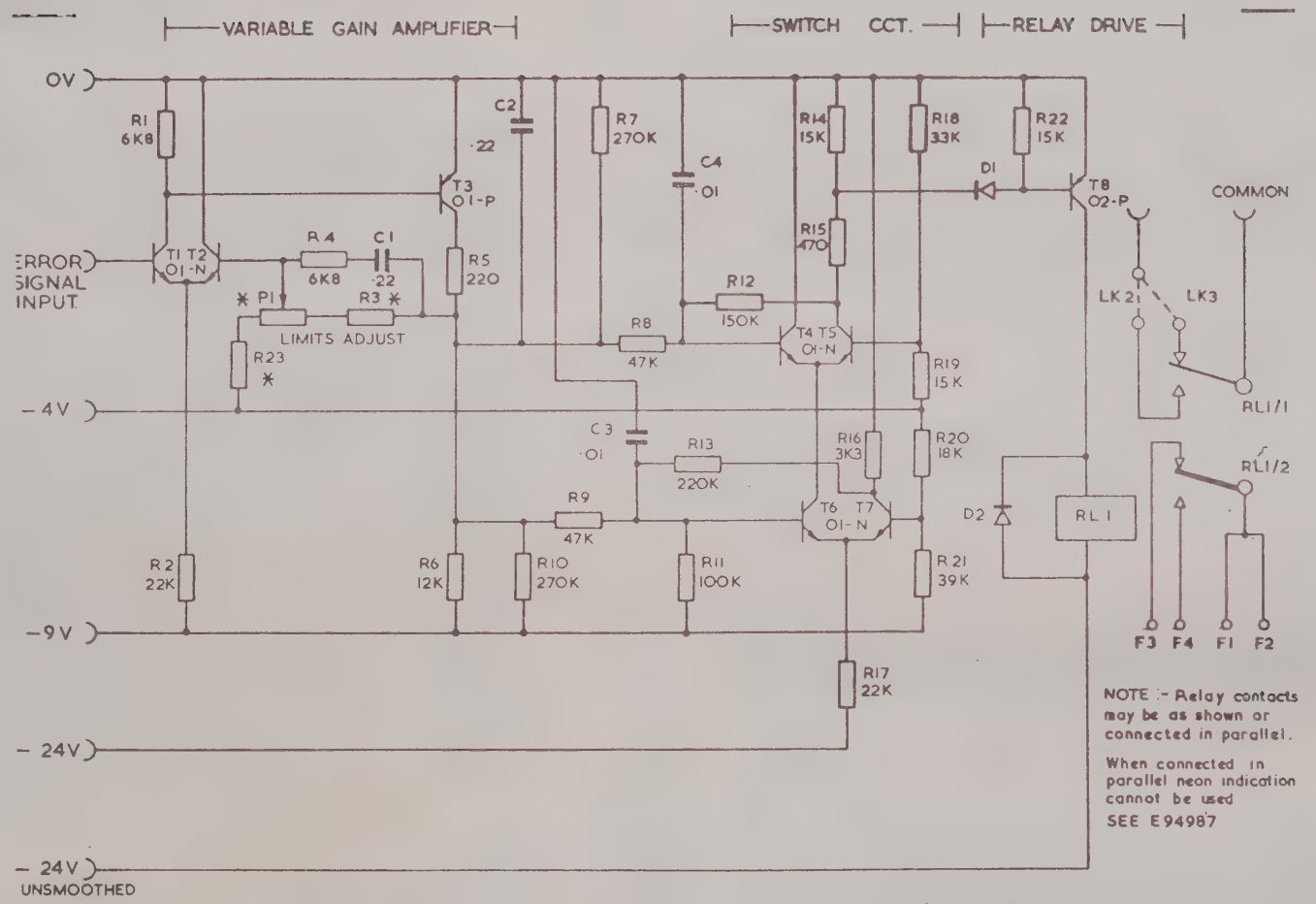
1. With the limits board and the main amplifier board inserted in the mother board, connect the mains supply and check the -24V, -28V, +24V, -4V and -9V supplies with a d.c. voltmeter. Failure of any of the power supplies could be due to a mother board fault.
2. Set the control temperature to a value approximately, mid-span and inject a corresponding signal into the thermocouple input from a millivolt source. With zero error, ensure that the relay is energised.
3. Set the limit alarm potentiometer P1 to approximately mid-way (5%). Slowly increase the injected millivolt signal to a value corresponding to 5% of span above the set point. Ensure that the relay de-energises at the alarm point.
4. Reduce the injected signal to a value corresponding to the set point. Check that the relay re-energises.
5. Reduce the injected signal to a value corresponding to 5% of span below the set point. Ensure that the relay de-energises at the alarm point.
6. Check limit alarm operation at the two extremes settings of the limit potentiometer (1% and 10% of span) If the alarm is not functioning correctly, check the operation of T1, T2 and T3 with reference to the d.c. voltage table. If no fault is indicated check the operation of T4 to T8.

D.C. Voltage Table.

Typical d.c. test voltages for the transistors are shown in the table. All voltages are measured with reference to 0V using a d.c. voltmeter having a resistance of 20K /Volt. The limit control P1 must be set to the maximum, fully clockwise position (10%). Voltages are checked with the indicator upscale (maximum over temperature error), downscale (maximum under temperature error) and at the set point (zero error).

	INDICATOR POSITION	T1	T2	T3	T4	T5	T6	T7	T8
EMITTER	Upscale (max.error)	-7	-7	0	0	0	-6	-6	0 V
	Set Point (zero error)	-4.5	-4.5	0	-3	-3	-5.5	-5.5	0 V
	Downscale (max.error)	-2.5	-2.5	0	-2	-2	-4	-4	0 V
BASE	Upscale	-6.5	-6	-ve	-4	-2.5	-6	-5.5	-ve V
	Set Point	-4	-4	-0.5	-3	-2.5	-4	-5.5	-0.7 V
	Downscale	-2	-2	-0.5	-1	-2.5	-3	-5.5	0 V
COLLECTOR	Upscale	-ve	0	-6.5	0	-0.5	0	-3	-21 V
	Set Point	-0.5	0	-4	0	-2	-3	-ve	0 V
	Downscale	-0.5	0	-1.5	0	-ve	-2	-ve	-19 V

Points designated only '-ve' are close to zero but slightly negative.



NOTE :- Relay contacts may be as shown or connected in parallel.

When connected in parallel neon indication cannot be used

SEE E94987

COMPONENTS MARKED THUS * VARY WITH RANGE
SEE WRITE UP FOR DETAILS
LAYOUT Nº E94987

E92111 Sht 26

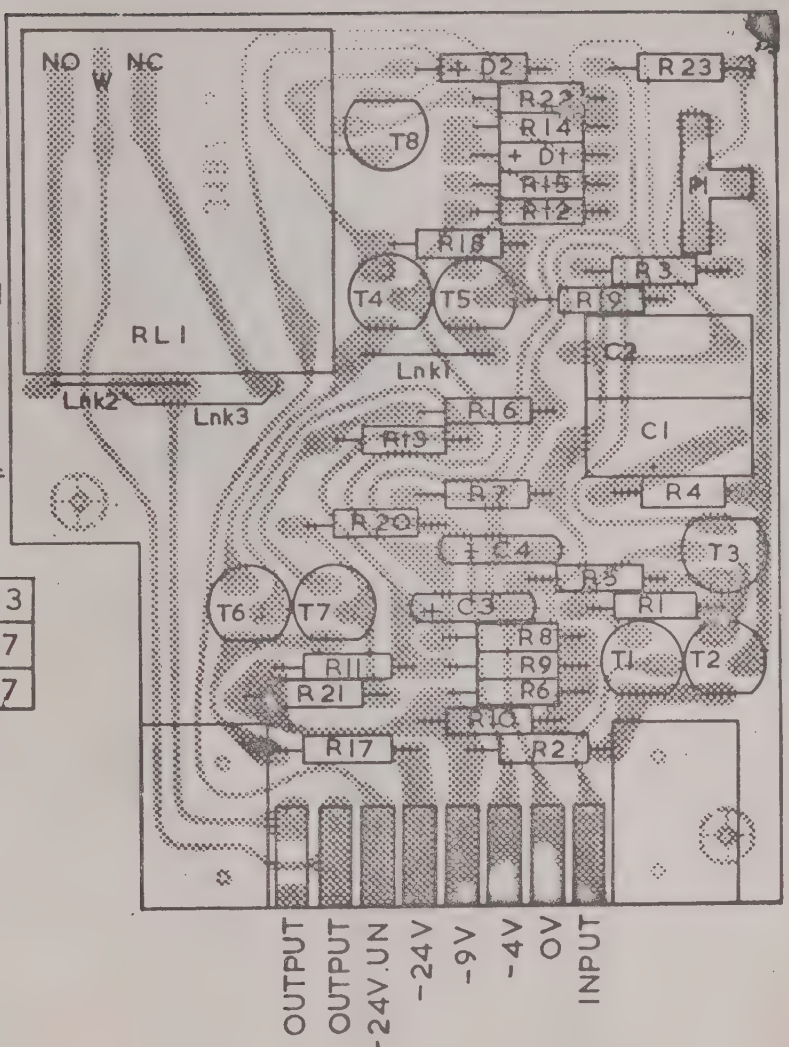
017/ 018 Series.
ALL LIMITS BOARD
with NEON INDICATION.

CONTACTS CLOSING
IN ALARM CONDITION
ADD LINK 3
OMIT LINK 2

CONTACTS OPENING
IN ALARM CONDITION
ADD LINK 2.
OMIT LINK 3

CIRCUIT Nº E92111 sht 9

RANGE	PI	R3	R23
0·5–5%	22K	33K	2K7
1–10%	22K	5K6	2K7



LILLIPUT MkII.
ALL LIMITS.

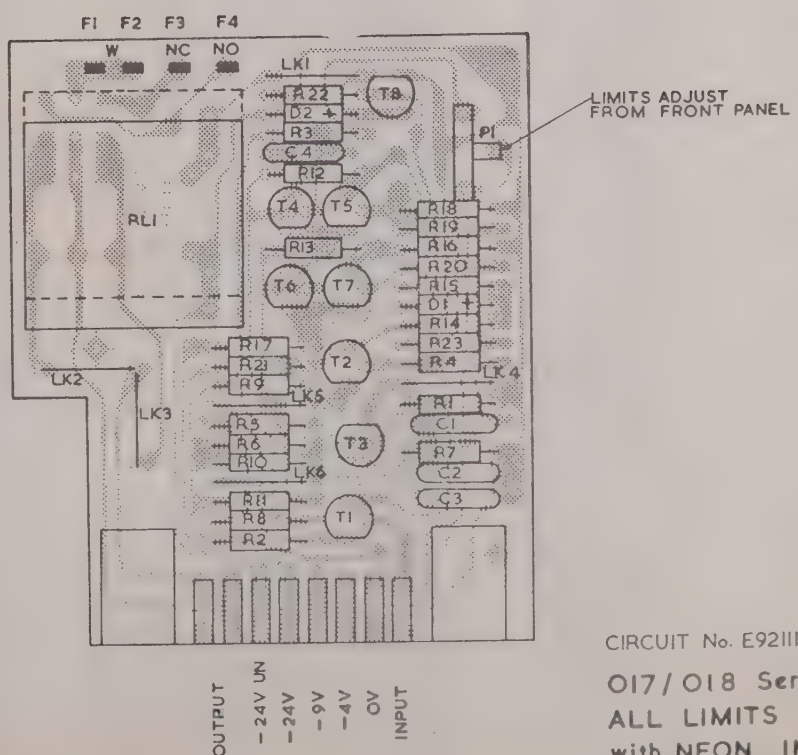
Drg Nº D93261

NOTE: WITH RELAY IN LOWER POSITION CONTACTS ARE CONNECTED IN PARALLEL, WITH RELAY IN UPPER POSITION ONE SET OF CONTACTS MAY BE USED FOR ALARM INDICATION.

CONTACTS CLOSING IN ALARM CONDITION ADD LINK 3
OMIT LINK 2

CONTACTS OPENING IN ALARM CONDITION ADD LINK 2
OMIT LINK 3

RANGE	PI	R3	R23
0·5-5%	22K	33K	2K7
1-10%	22K	5K6	2K7



CIRCUIT No. E92111. Sht.26.

017/018 Series
ALL LIMITS BOARD
with NEON INDICATION

Drg.No. E94987

TIME PROPORTIONING HIGH LIMIT (Option 67)

Function

This limit board provides a set of relay contacts which operate in a time proportioning mode with a fixed 4% proportional band. The lower limit of the proportional band can be adjusted by P1 over a range of either -6 to +2% or 0 to 5% of span. Because this action operates from the error signal and not the control signal it is proportional only. The cycle time at 50% power is 12 sec on +12 sec off and is proportional to C4.

Circuit Description.

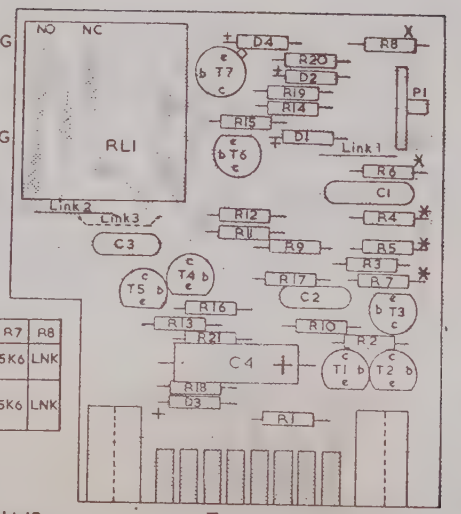
The output of the error amplifier is applied to the input of the amplifier T1, T2, T3, and associated components. The output voltage of which can be varied by adjustment of P1. The output voltage at the junction of R9 and R10 is applied to the base of T4 which with T5, T6 and associated components provides the time proportioning action. The output at T6 collector is fed to the base of T2 by R5. Components C1 and R3 form a high frequency filter. The output from this stage, at the junction of R9 and R10, is applied to the base of T4 via R11. This will cause T4 to turn off, thus turning T6 off. T6 collector falls negative and feedback is applied to the base of T4 via R15 to ensure that T4 remains off. Since the collector of T6 is now at -9V, due to clamping action of D3, D1 is now forward biased and will permit C4 to charge negatively. When C4 has charged sufficiently negative to overcome the hysteresis introduced by R15, T4 will switch back on, turning T6 on. The feedback introduced by R15 ensures that T4 remains on. T7 is now switched off due to the rise in collector potential at T6. The cycle is then repeated.

Checking.

1. With the limit board plugged into the instrument check the voltage supplies to the board.
2. Set the control temperature to a value corresponding to mid-span and inject the appropriate mV. Check that the relay cycles as the input mV signal is varied through the proportional band. Depending upon the range of the board with P1 set clockwise the time proportioning action may be observed as the mV input is raised or as the set point is lowered about the mid-span value.

* CONTACTS CLOSING FOR HIGH TEMP.
ADD LINK 2
OMIT LINK 3

CONTACTS OPENING FOR HIGH TEMP.
ADD LINK 3
OMIT LINK 2



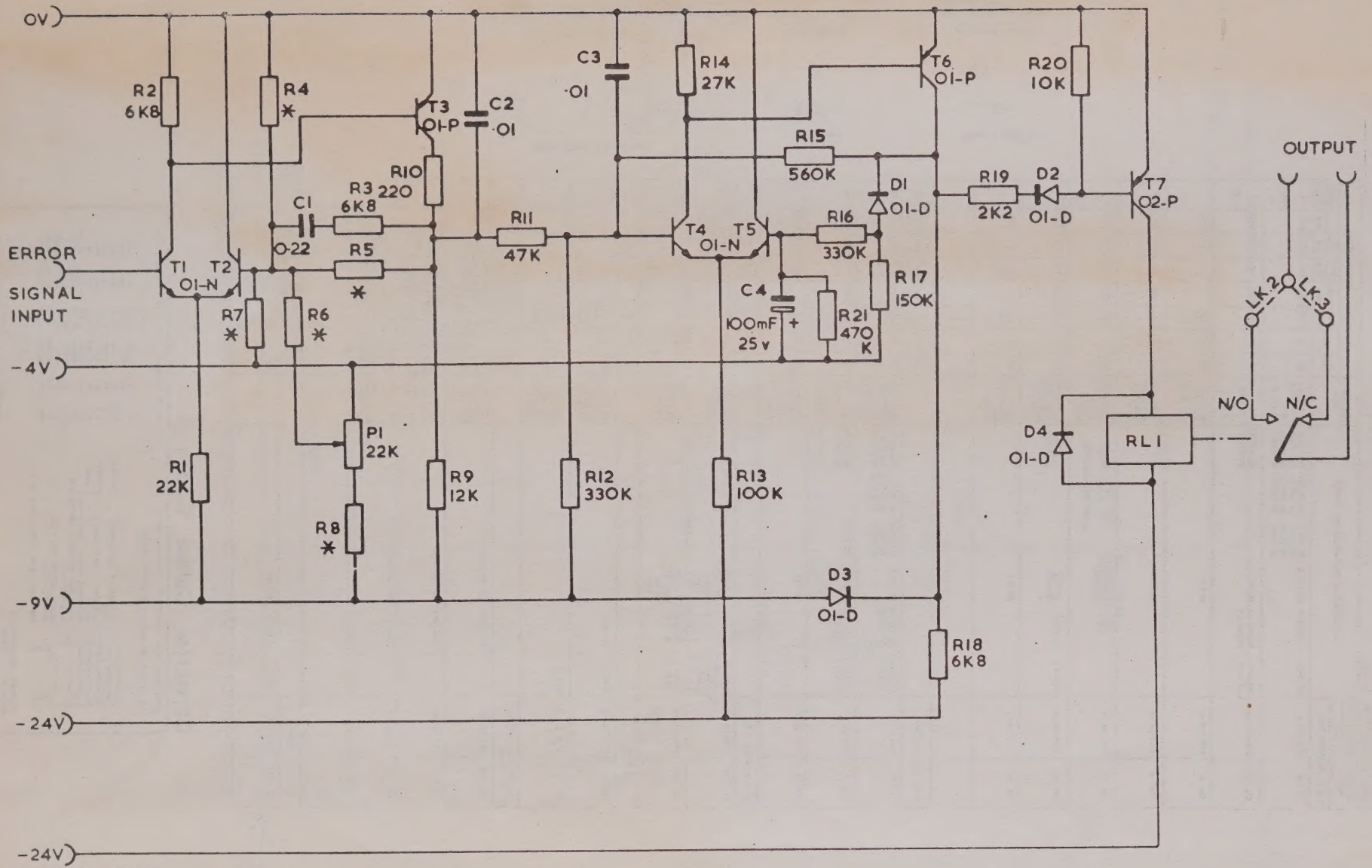
RANGE	R4	R5	R6	R7	R8
4% PROP. 0-5% SP'N	—	27K	39K	5K6	LNK
* 4% PROP. -6 TO +2% SPAN.	33K	27K	33K	5K6	LNK

CIRCUIT N° E92111 Sht 18.

* PREFERRED OPTION.

Drg N° D93925

LILLIPUT Mk II
T.P.H.L.



COMPONENTS MARKED THUS * VARY WITH RANGE.
SEE WRITE UP FOR DETAILS.
LAYOUT Nº D93925

LILLIPUT Mk II.
TIME PROPORTIONING
HIGH LIMIT.

E92111 Sht18

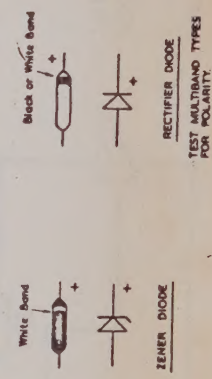
SEMICONDUCTOR TABLE

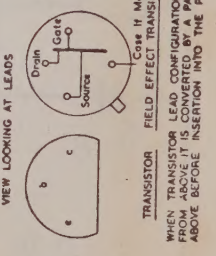
CIRCUIT REF	PT No./STORES REF INCLUDES PAD	ACCEPTABLE REPLACEMENT TYPES	DESCRIPTION	ABRIDGED SPECIFICATION							
				VCEO	VEBO	Hfe 2mA MIN.	Hfe 2mA MAX.	Hfe 10µA MIN.	IC MAX. mA	P tot mW	NOISE FACTOR
NPN TRANSISTORS											
Q1 - N	TRN Q1 - N	BC168B BC183LB BC172B BC167B BC182LB BC548B BC168C BC182LC BC147B BC169B BC184LB BC148B BC169C BC184LC BC238B	GENERAL PURPOSE NPN PLASTIC	20	5	240	500	80	200	200	4 (<10)
Q2 - N	TRN Q2 - N	BC167A BC182LA BC171B BC237B BC167B BC182LB BC547B	HIGH VOLTAGE NPN PLASTIC	45	6	125	500	40	200	200	4 (<10)
Q3 - N	TRN Q3 - N	BFY51	MEDIUM POWER NPN TO5	60	6	40 (150 mA)			1A	800	
Q4 - N	TRN Q4 - N	BC131B	LOW NOISE NPN TO18 MEDIUM GAIN	20	5	240	500	80	200	200	< 4
Q5 - N	TRN Q5 - N	BC131C BC130C BC109C* *CAN NOT ISOLATED	LOW NOISE NPN TO18 HIGH GAIN	20	5	450	900	100	200	135	< 4 <10
Q6 - N	TRN Q6 - N	BC169C BC184C BC172C BC239C BC149C BC549C	LOW NOISE NPN PLASTIC MED HIGH GAIN	20	5	240	900	80	200	200	< 4
Q7 - N	TRN Q7 - N	BD124	HIGH POWER NPN SO. 55	45	6	25 (2A)		25 (50 mA)	4A	15W	
PNP TRANSISTORS				VCEO	VEBO	Hfe 2mA MIN.	Hfe 2mA MAX.	Hfe 10µA MIN.	IC MAX. mA	P tot mW	N.F.
Q1 - P	TRN Q1 - P	BC258A BC213LB BC251B BC257A BC212LB BC307B BC258B BC213LC BC259A BC214LB BC308B BC259B BC214LC BC558B	GENERAL PURPOSE PNP PLASTIC	25	5	125	600	40	200	200	< 10
Q2 - P	TRN Q2 - P	BC257B BC212LA BC251B BC307B BC557B BC257A BC212B BC157B BC261B	HIGH VOLTAGE PNP PLASTIC	45	5	75	400	30	200	200	<10
Q3 - P	TRN Q3 - P	BFX87	MEDIUM POWER PNP TO5	50	4	40 10mA			600	600	
N - CHANNEL F.E.T.				VDS	VDG	VGS MAX.	IG	IGSS VDS =0	VGS		
Q1 - NF	TRN Q1 - NF	U2122E (SELECT FROM 2N4303) WN080 (SELECT FROM E102)	F.E.T. PLASTIC TO 18	30	30	20	10	1nA VGS = -10	VGS @ ID = 200µA MIN 1V	MAX. 2.5V	
Q2 - NF	TRN Q2 - NF	2N4221 SELECT 2N3822 SELECT WN080 (SELECT FROM E102)	F.E.T. LOW LEAKAGE TO 18	30	30	30		100 pA VGS = -15			
DIODES				PIV	IAV	IR					
D1 - D	D 1O Q1 - D	BAX 16 IS922	GENERAL PURPOSE GLASS DIODE	150	200	0.1 µA @ 150 P.I.V.					
D2 - D	D 1O Q2 - D	BYX 10	HIGH VOLTAGE PLASTIC RECTIFIER DIODE	800	360	50 µA @ 800 P.I.V.					
REFERENCE (ZENER) DIODES				VZ VOLTS			rz Ω		P TOT		
				MIN	TYP.	MAX	TYP	MAX.			
5.6 - DZ	DIZ 5.6 - DZ	IS2056A BZY88 C5V6	IZ = 1mA	4.8	5.3	5.8	160	350	400 mW		
			IZ = 5mA	5.3	5.6	6.0	15	55			
			IZ = 20mA	5.4	5.7	6.1	3.5	8			
6.2 - DZ	DIZ 6.2 - DZ	IS2062A BZY88 C6V2	IZ = 1mA	5.7	5.9	6.5	29	250	400 mW		
			IZ = 5mA	5.8	6.2	6.6	5	27			
			IZ = 20mA	5.9	6.4	6.7	2.5	3.1			
8.2 - DZ	DIZ 8.2 - DZ	IS082A BZY88 C8V2	IZ = 1mA	7.8	8.1	8.6	8.5	20	400 mW		
			IZ = 5mA	7.8	8.2	8.7	4	20			
			IZ = 20mA	7.9	8.4	8.9	2	6			
TRIGGER DIODE				BREAKDOWN VOLTS		MIN V BREAKBACK		PEAK I Amp			
D1 - DT	DIA.D1 - DT	ST. 2 TIC 54 BR100		32 ± 4		4		1			

T2

T1, T2

DIAC



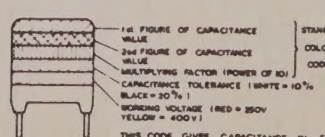


WHEN TRANSISTOR LEAD CONFIGURATION DIFFERS FROM ABOVE IT IS CONVERTED BY A PAD TO THE ABOVE BEFORE INSERTION INTO THE P.C.B.

Capacitor Colour Codes

METALLISED FILM CAPACITORS - COLOUR CODE

THE METHOD OF MARKING IS SHOWN BELOW:-

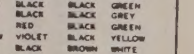

1st FIGURE OF CAPACITANCE VALUE
2nd FIGURE OF CAPACITANCE VALUE
MULTIPLYING FACTOR (POWER OF 10)
CAPACITANCE TOLERANCE (WHITE = 10%, BLACK = 20%)
WORKING VOLTAGE (RED = 250V, YELLOW = 400V)
STANDARD COLOUR CODE

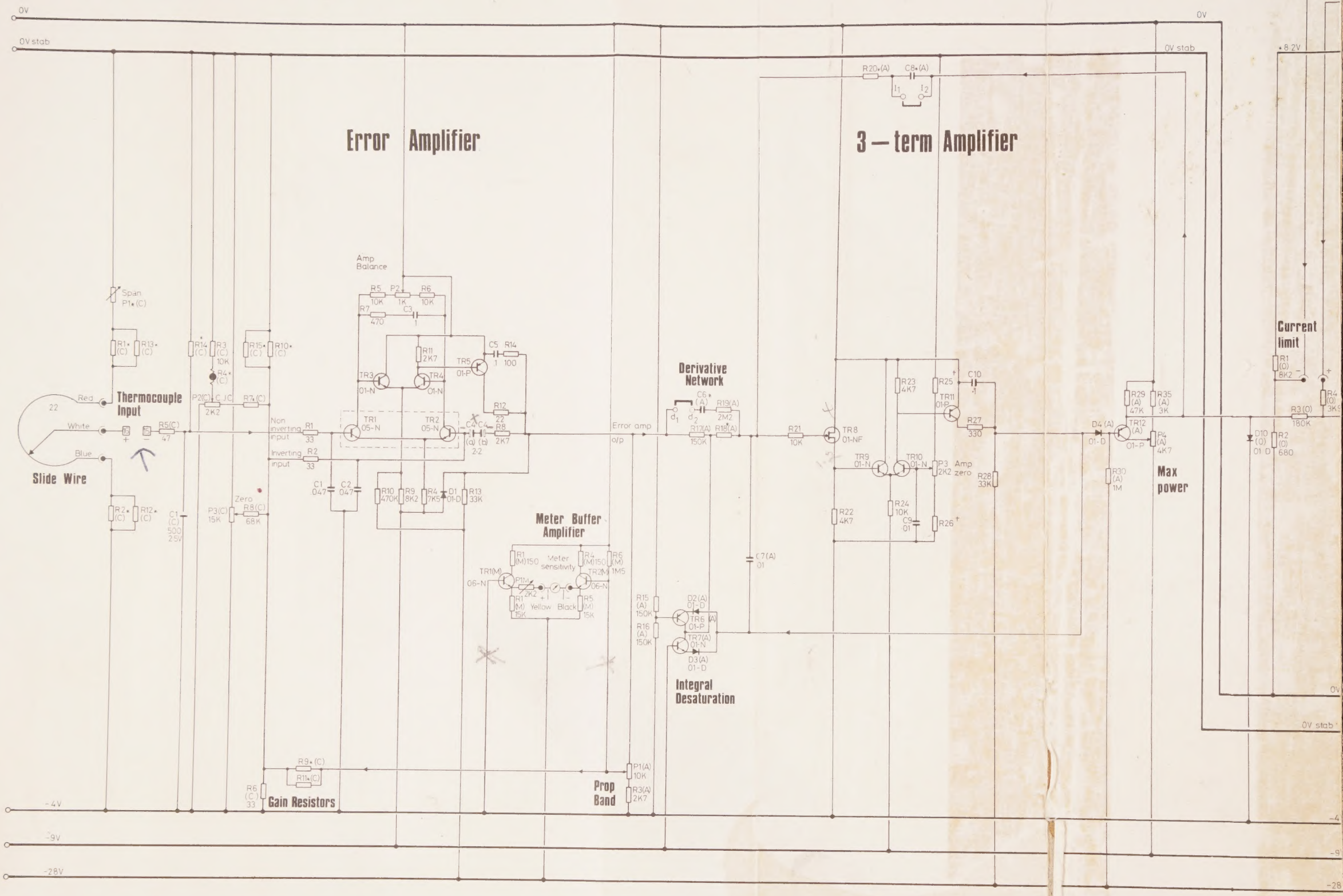
THIS CODE GIVES CAPACITANCE IN pF

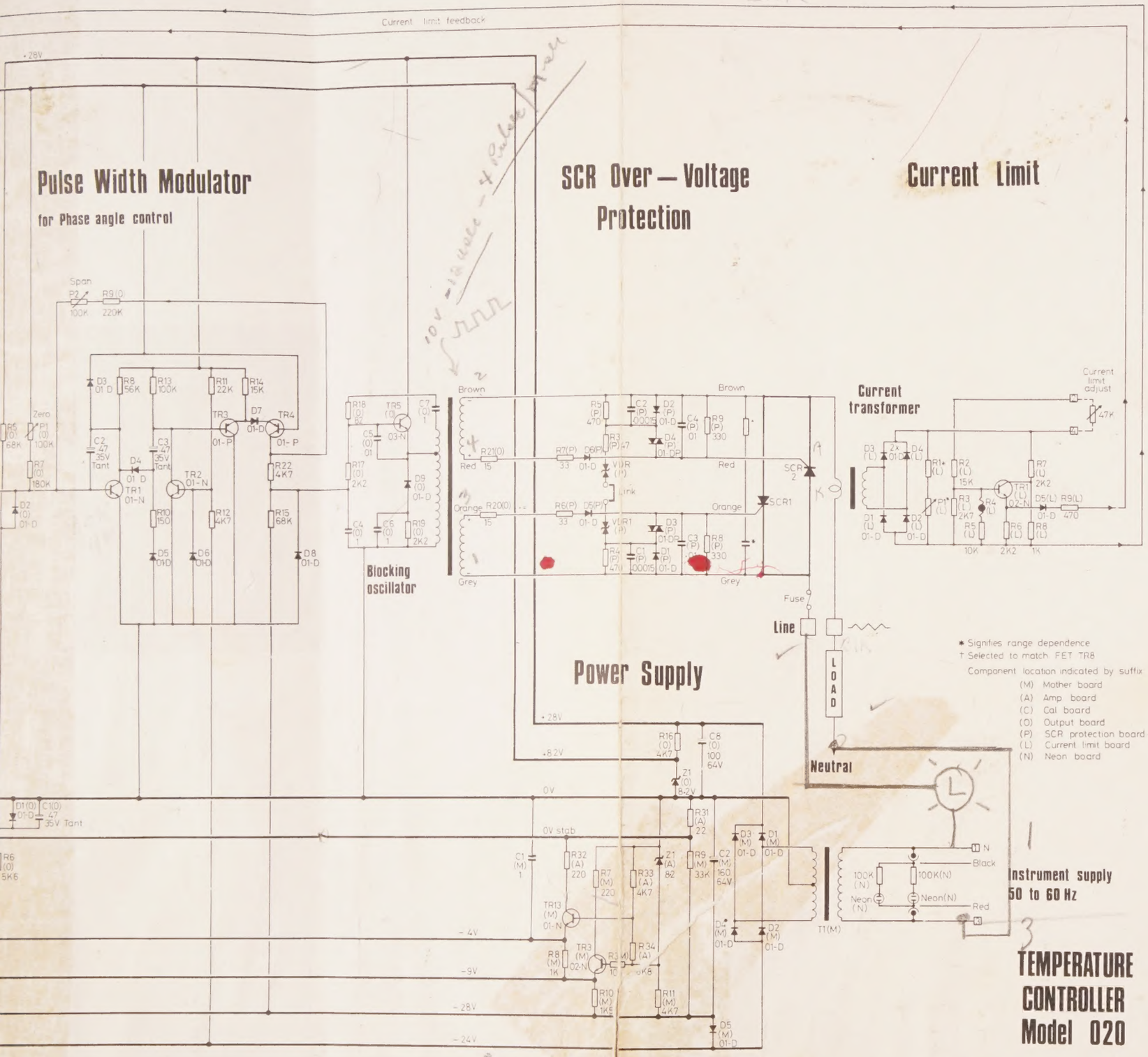
STANDARD COLOUR CODE			
BLACK = 0	GREEN = 5		
BROWN = 1	BLUE = 6		
RED = 2	VIOLET = 7		
ORANGE = 3	GREY = 8		
YELLOW = 4	WHITE = 9		

SOLID TANTALUM CAPACITORS - COLOUR CODE

µF	V	COLOUR CODE			
0.1	35	BROWN	BLACK	GREY	PINK
0.22	35	RED	RED	GREY	PINK
0.47	35	YELLOW	VIOLET	GREY	PINK
1.0	35	BROWN	BLACK	WHITE	PINK
2.2	35	RED	RED	WHITE	PINK
4.7	35	YELLOW	VIOLET	WHITE	PINK
10	6.3	BROWN	BLACK	BLACK	YELLOW
10	16	BROWN	BLACK	BLACK	GREEN
10	25	BROWN	BLACK	BLACK	GREY
22	16	RED	RED	BLACK	GREEN
47	6.3	YELLOW	VIOLET	BLACK	YELLOW
100	3.0	BROWN	BLACK	BROWN	WHITE




0V
0V stab
+8.2V
-4V
-9V
-28V
Error Amplifier
3 — term Amplifier
Span
P1*(C)
Thermocouple Input
Red
White
Blue
Slide Wire
Amp Balance
Non inverting input
Inverting input
Error amp o/p
Derivative Network
Meter Buffer Amplifier
Meter sensitivity
Yellow
Black
Integral Desaturation
Current limit
Max power
Amp zero
Zero
Gain Resistors
Prop Band



SCR

L1 ○ ○ Ground

Lamp

L2

D3 } Diac

D4 } EK 561-2570-320